datasheet

PRELIMINARY SPECIFICATION

1/2.9" color CMOS 2 megapixel image sensor

OS02G10

color CMOS 2 megapixel image sensor

datasheet (CSP)
PRELIMINARY SPECIFICATION

version 1.11
october 2020

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applications

- security surveillance systems
- IP cameras
- HD analog cameras

ordering information

- **OS02G10-A41A-001A-Z** (color, lead-free)
  41-pin CSP

features

- programmable controls: frame rate, mirror and flip, cropping, and windowing
- supports 2x2 color binning function
- supports output formats: 12-bit/10-bit RAW RGB
- SCCB control interface for register programming
- supports MIPI 2-lane serial output interface
- supports DVP 12-bit output interface
- supports image sizes:
  1920 x 1080 @ 30 fps
- supports automatic black level calibration
- supports multi-camera synchronous function

key specifications (typical)

- **active array size:** 1920 x 1080
- **power supply:**
  analog: 2.8V
  I/O: 1.8V
  core: 1.5V
- **power requirements:** (see **sidebar note**)
  active: TBD
  standby: TBD
- **temperature range:**
  operating: -30°C to +85°C junction temperature (see **table 6-2**)
  stable image: -20°C to +60°C junction temperature (see **table 6-2**)
- **output interfaces:** MIPI 2-lane/DVP 12-bit
- **output formats:** RAW RGB
- **lens size:** 1/2.9"
- **lens chief ray angle:** 15° linear (see **figure 8-3**)
- **input clock frequency:** 10~36 MHz
- **maximum image transfer rate:**
  1920 x 1080: 30 fps
- **sensitivity:** TBD
- **shutter:** rolling
- **max S/N ratio:** TBD
- **dynamic range:** TBD
- **pixel size:** 2.8 µm x 2.8 µm
- **image area:** 6417 µm x 4145 µm
- **package dimensions:** 6451 µm x 4179 µm

note Power requirements specifications are estimated values and are subject to change when measured data using real silicon is available.

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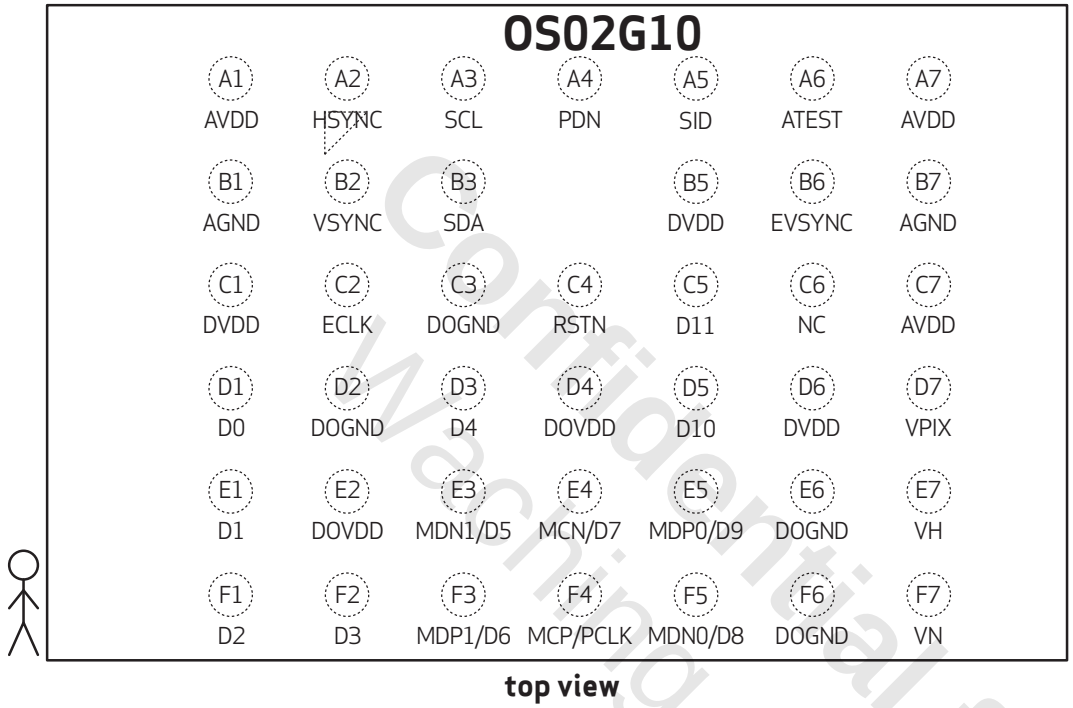
1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OS02G10 image sensor. The package information is shown in **section 8**.

figure 1-1 pin diagram



top view

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	AVDD	power	analog power 2.8V
A2	**HSYNC**	output	horizontal sync signal
A3	**SCL**	input	SCCB clock
A4	**PDN**	input	power down 0: Enable 1: Normal work
A5	**SID**	input	SID control
A6	ATEST	output	analog test output

table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
A7	AVDD	power	analog power 2.8V
B1	AGND	ground	analog ground
B2	**VSYNC**	output	vertical sync signal
B3	**SDA**	I/O	SCCB data
B5	DVDD	power	digital core power 1.5V
B6	**EVSYNC**	I/O	external vertical sync signal
B7	AGND	ground	analog ground
C1	DVDD	power	digital core power 1.5V
C2	**ECLK**	input	external clock input
C3	DOGND	ground	digital ground
C4	**RSTN**	input	reset 0: Enable 1: Normal work
C5	**D11**	output	DVP data output 11
C6	NC	–	no connect
C7	AVDD	power	analog power 2.8V
D1	**D0**	output	DVP data output 0
D2	DOGND	ground	digital ground
D3	**D4**	output	DVP data output 4
D4	DOVDD	power	digital I/O power 1.8V/2.8V
D5	**D10**	output	DVP data output 10
D6	DVDD	power	digital core power 1.5V
D7	VPIX	output	internal reference (connect to 1µF capacitor outside)
E1	**D1**	output	DVP data output 1
E2	DOVDD	power	digital I/O power 1.8V/2.8V
E3	**MDN1/D5**	output	MIPI data negative output 1 output and DVP data output 5
E4	**MCN/D7**	output	MIPI clock negative output and DVP data output 7
E5	**MDP0/D9**	output	MIPI data positive output 0 and DVP data output 9
E6	DOGND	ground	digital ground
E7	VH	reference	internal reference (connect to 1µF capacitor outside)
F1	**D2**	output	DVP data output 2

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
F2	**D3**	output	DVP data output 3
F3	**MDP1/D6**	output	MIPI data positive output 1 and DVP data output 6
F4	**MCP/PCLK**	output	MIPI clock positive output and pixel output clock
F5	**MDN0/D8**	output	MIPI data negative output 0 and DVP data output 8
F6	DOGND	ground	digital ground
F7	VN	reference	internal reference (connect to 1µF capacitor outside)

table 1-2 pin states under various conditions (sheet 1 of 2)

pin number	signal name	PDN = 0	PDN = 1; RSTN = 0	PDN = 1; RSTN = 1
A2	HSYNC	high-z	high-z	high-z by default (configurable)
A3	SCL	high-z	input	input
A4	PDN	input	input	input
A5	SID	input	input	input
B2	VSYNC	high-z	high-z	high-z by default (configurable)
B3	SDA	high-z	high-z	I/O
B6	EVSYNC	high-z	high-z	I/O (configurable)
C2	ECLK	input	input	input
C4	RSTN	input	input	input
C5	D11	high-z	high-z	high-z by default (configurable)
D1	D0	high-z	high-z	high-z by default (configurable)
D3	D4	high-z	high-z	high-z by default (configurable)
D5	D10	high-z	high-z	high-z by default (configurable)
E1	D1	high-z	high-z	high-z by default (configurable)
E3	MDN1/D5	high-z	high-z	high-z by default (configurable)
E4	MCN/D7	high-z	high-z	high-z by default (configurable)
E5	MDP0/D9	high-z	high-z	high-z by default (configurable)
F1	D2	high-z	high-z	high-z by default (configurable)
F2	D3	high-z	high-z	high-z by default (configurable)

table 1-2 pin states under various conditions (sheet 2 of 2)

pin number	signal name	PDN = 0	PDN = 1; RSTN = 0	PDN = 1; RSTN = 1
F3	MDP1/D6	high-z	high-z	high-z by default (configurable)
F4	MCP/PCLK	high-z	high-z	high-z by default (configurable)
F5	MDN0/D8	high-z	high-z	high-z by default (configurable)

table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

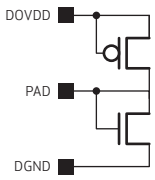
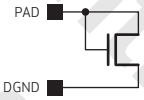
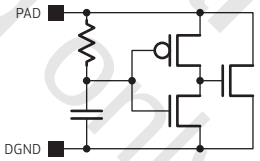
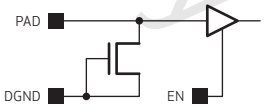
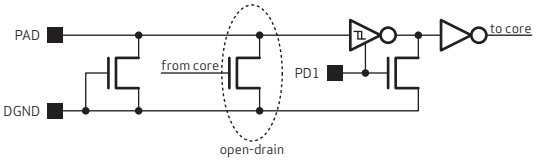
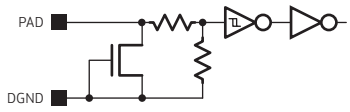
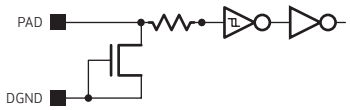
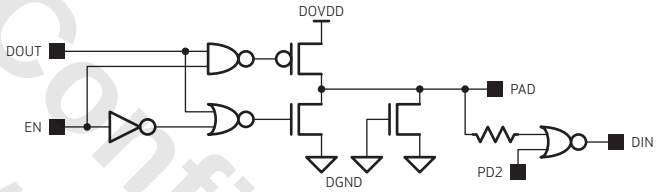
symbol	equivalent circuit
D0, D1, D2, D3, D4, MDN1/D5, MDP1/D6, MCN/D7, MCP/PCLK, MDN0/D8, MDP0/D9, D10, D11	
AGND, DGND, VPIX, ATEST, VH	
VN	
AVDD, DVDD, DOVDD	
ECLK	
SDA	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
RSTN, PDN	
SCL	
EVSYNC	

2 system level description

2.1 overview

The OS02G10 image sensor is a high quality, 1/2.9 inch, 1080p format, CMOS image sensor. It provides high quality digital images and high-definition (HD) video. The OS02G10 focuses on products including security surveillance systems, IP cameras and HD analog cameras.

By introducing an advanced 2.8 µm pixel architecture, the OS02G10 achieves excellent low-light sensitivity, signal-to-noise ratio, full-well capacity, quantum efficiency and low-power consumption. The default mode and programmable mode allow for a more convenient way of controlling the parameters of frame size, exposure time, gain value, etc. It also offers the following image control functions: mirror and flip, windowing, auto black level calibration, defective pixel correction, black sun cancellation, and other functions.

The OS02G10 supports a high frame rate of up to 30 fps @ 1080p format through the DVP interface or MIPI interface. These prominent features integrated in the OS02G10 allow for a best-in-class image sensor that will bring users vivid pictures and an excellent experience.

2.2 architecture

The OS02G10 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OS02G10 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre-charging and sampling the rows of the array sequentially. In the time between pre-charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs up to 10-bit data for each pixel in the array.

figure 2-1 OS02G10 block diagram

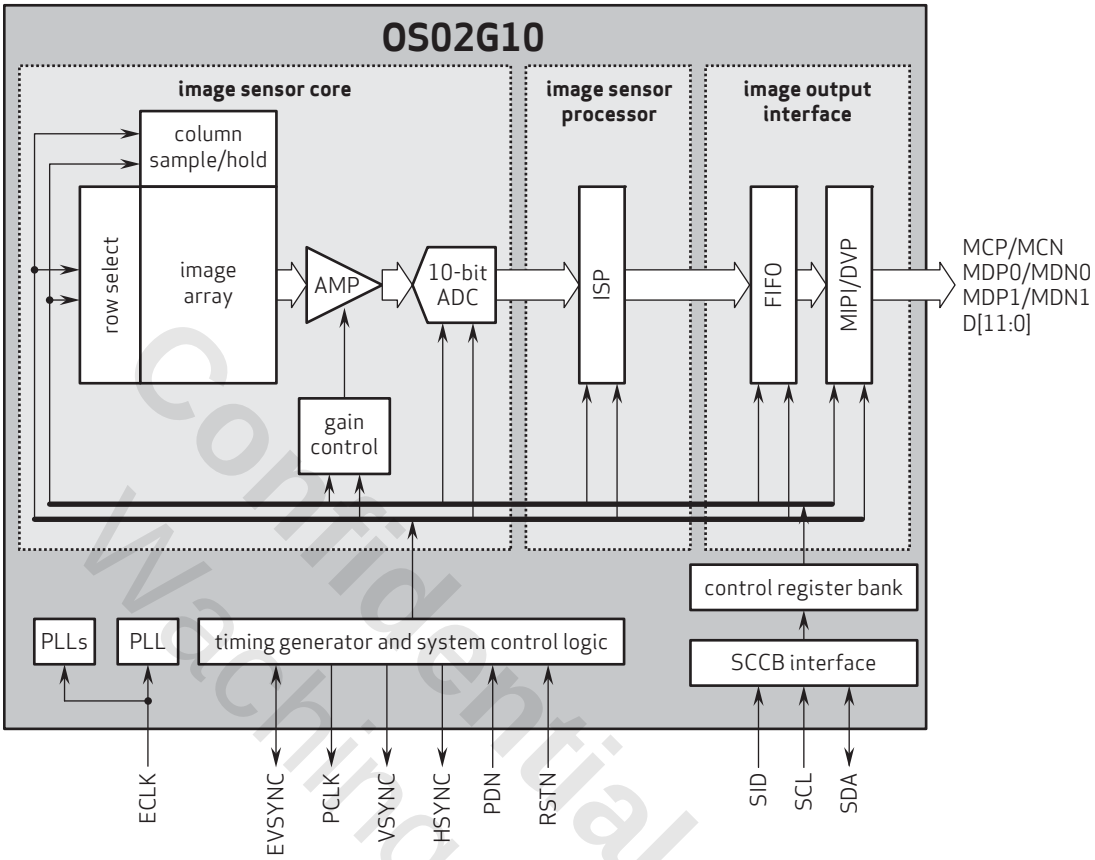
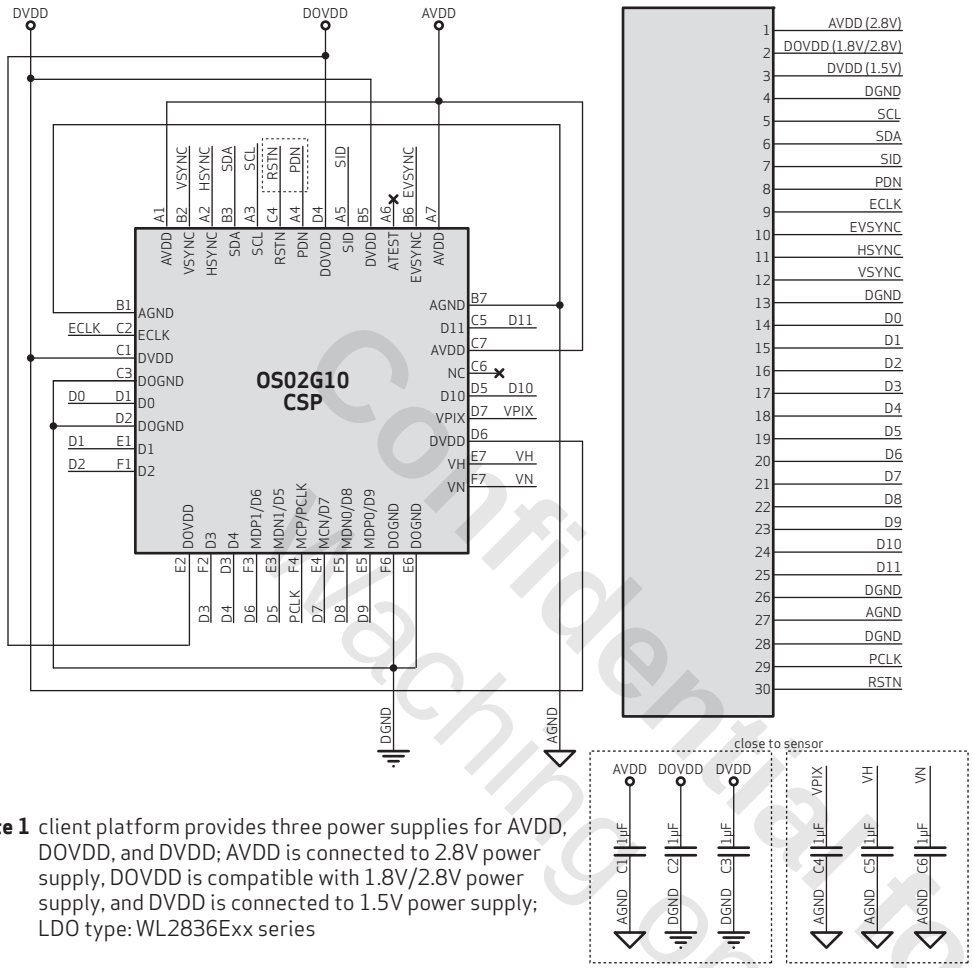


figure 2-2 OS02G10 DVP reference schematic



note 1 client platform provides three power supplies for AVDD, DOVDD, and DVDD; AVDD is connected to 2.8V power supply, DOVDD is compatible with 1.8V/2.8V power supply, and DVDD is connected to 1.5V power supply; LDO type: WL2836Exx series

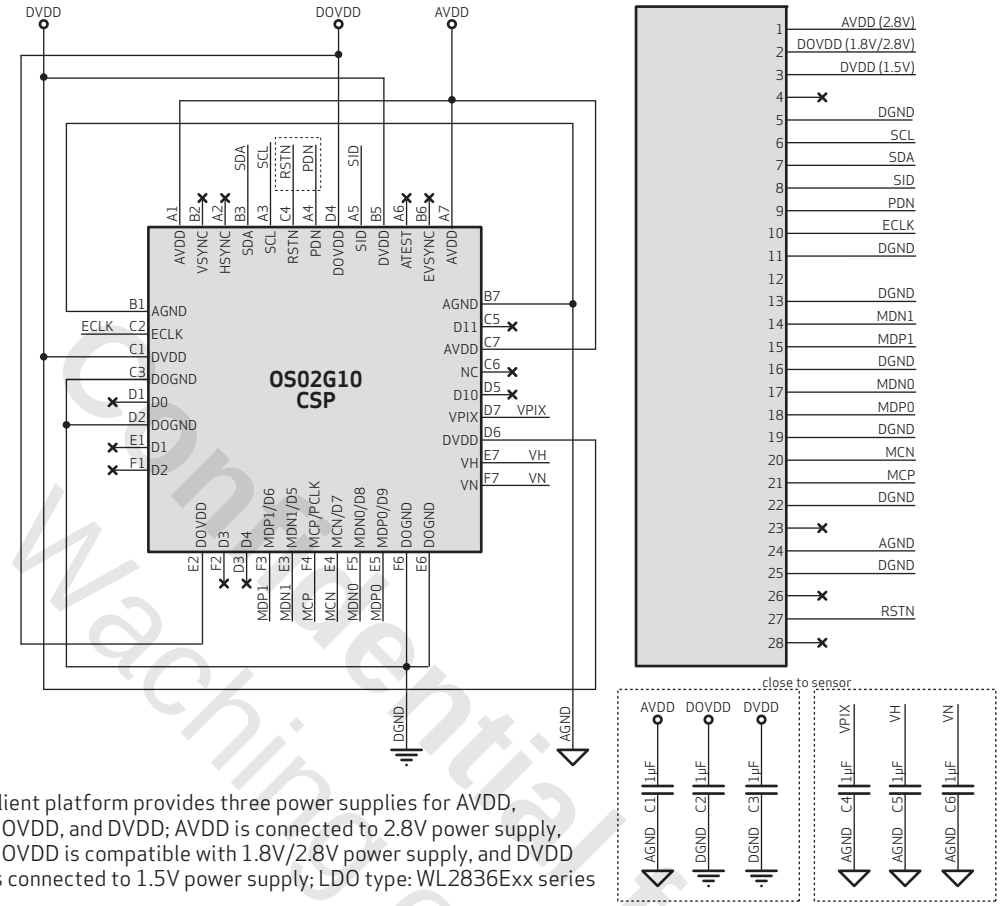
note 2 when platform GPIO pin is limited, PDN must be controlled by platform GPIO; RSTN can be directly connected to DOVDD

note 3 this design is for parallel port mode, where MDN1/D5, MDP1/D6, MDN0/D8, MDP0/D9, MCN/D7, and MCN/PCLK are multiplexed pins, and are used as D5, D6, D8, D9, D7 and PCLK; SID is SCCB address controllable pin; when SID is connected low, write address is 0x78 and read address is 0x79; when SID is connected high, write address is 0x7A and read address is 0x7B

note 4 in PCB design, place chip power filter capacitors close to power pins; place 1 μF capacitors near AVDD, DOVDD, DVDD, VPIX, VH, VN in module; AGND and DGND of sensor should be separated inside module and outside PCB single-point connection; AVDD and AGND should not be adjacent to clock; power supply should be designed as thin as 0.12 mm as much as possible, and bottom line should be pulled to ground

note 5 FPC using anti-jamming design

figure 2-3 OS02G10 MIPI reference schematic



note 1 client platform provides three power supplies for AVDD, DOVDD, and DVDD; AVDD is connected to 2.8V power supply, DOVDD is compatible with 1.8V/2.8V power supply, and DVDD is connected to 1.5V power supply; LDO type: WL2836Exx series

note 2 when platform GPIO pin is limited, PDN must be controlled by platform GPIO; RSTN can be directly connected to DOVDD

note 3 this design is for MIPI mode, where MDN1/D5, MDP1/D6, MDN0/D8, MDP0/D9, MCN/D7, and MCN/PCLK are multiplexed pins, and are used as MDN1, MDP1, MDN0, MDP0, and MCN and MCP; SID is SCCB address controllable pin; when SID is connected low, write address is 0x78 and read address is 0x79; when SID is connected high, write address is 0x7A and read address is 0x7B

note 4 in PCB design, place chip power filter capacitors close to power pins; place 1 µF capacitors near AVDD, DOVDD, DVDD, VPIX, VH, VN in module; AGND and DGND of sensor should be separated inside module and outside PCB single-point connection; AVDD and AGND should not be adjacent to clock; power supply should be designed as thin as 0.12 mm as much as possible, and bottom line should be pulled to ground

note 5 MCN/MCP, MDN0/MDP0, and MDN1/MDP1 are three pairs of differential lines; traces should be wrapped as long as possible with equal spacing; bottom layer (or top layer) of differential lines must have a complete reference ground; for PCB manufacturers to distinguish which are differential lines, manufacturers need to perform impedance control during production; impedance standard is 100 ohm, and error cannot exceed ±10%

note 6 FPC using anti-jamming design

2.3 format and frame

The OS02G10 supports RAW RGB output with a 2-lane MIPI interface.

table 2-1 formats and frame rates

format	resolution	frame rate	methodology	10-bit output MIPI data rate	DVP pixel clock
1080p	1920 x 1080	30 fps	full resolution qualified pixel (1920+8) x (1080+8)	2-lane @720 Mbps/lane 10-bit MIPI	36 MHz x 2
binning	968 x 548	60 fps	binning qualified pixel (960+4) x (540+4)	2-lane @720 Mbps/lane 10-bit MIPI	36 MHz x 2
720p	1280 x 720	60 fps	crop from full resolution	2-lane @720 Mbps/lane 10-bit MIPI	42 MHz x 2

2.4 readout drive mode

table 2-2 lists the operating modes available with the OS02G10 sensor.

table 2-2 operating modes

drive mode	timer clock (MHz)	frame rate (fps)	output resolution (bit)	data rate (Mpixels/s)	number of effective pixels		data width		1H period (s)
					H (pixels)	V (lines)	H (timer_clk)	V (lines)	
full res	42	30	10	84	1928	1088	ROWTIME ({P1:0x41, P1:0x42})	FRMTIME ({P1:0x4E, P1:0x4F})	ROWTIME /timer_clk
binning	42	60	10	42	964	544	ROWTIME ({P1:0x41, P1:0x42})	FRMTIME ({P1:0x4E, P1:0x4F})	ROWTIME /timer_clk
720p	42	60	10	84	1288	728	ROWTIME ({P1:0x41, P1:0x42})	FRMTIME ({P1:0x4E, P1:0x4F})	ROWTIME /timer_clk
VGA	42	60	10	42	648	488	ROWTIME ({P1:0x41, P1:0x42})	FRMTIME ({P1:0x4E, P1:0x4F})	ROWTIME /timer_clk

2.5 I/O control

Some I/O pads of the OS02G10 sensor can be configured as inputs or outputs.

table 2-3 I/O control functions

function	register	description
PCLK_INV_BUF, EVSYNC_OE_BUF, EVSYNC_IE, OUT_END_BUF, OUT_ENS_BUF, OUT_ENP_BUF	P0:0x1B	Bit[5]: pclk_inv_buf PCLK reverse enable 0: Disable PCLK reverse 1: Enable PCLK reverse Bit[4]: evsync_oe_buf Pad EVSYNC output enable signal 0: Enable output 1: Disable output Bit[3]: evsync_ie Pad EVSYNC input enable signal 0: Enable output 1: Disable output Bit[2]: out_end_buf Pad DATAOUT[9:0] output enable signal 0: Enable output 1: Disable output Bit[1]: out_ens_buf Pad VSYNC and HSYNC output enable signal 0: Enable output 1: Disable output Bit[0]: out_enp_buf Pad PCLK output enable signal 0: Enable output 1: Disable output
DS_DATA, DS_PCLK, DS_HSYNC, DS_VSYNC	P0:0x1E	Bit[7:6]: ds_vsync Driver current select signal of pad VSYNC Bit[5:4]: ds_hsync Driver current select signal of pad HSYNC Bit[3:2]: ds_pclk Driver current select signal of pad PCLK Bit[1:0]: ds_data Driver current select signal of pad DATAOUT[9:0]

2.6 MIPI interface

The OS02G10 supports a uni-directional two-lane MIPI transmitter interface and is capable of a data transfer rate of up to 840 Mbps. When MIPI works normally, the typical data type is RAW10 and also supports RAW8 data format. The default data transmission is high speed (HS) transfer mode.

2.6.1 function related register configuration

table 2-4 MIPI function related registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0x8E	H_SIZE_MIPI_4MSB	0x07	RW	Bit[3:0]: h_size_mipi[11:8]
P1:0x8F	H_SIZE_MIPI_8LSB	0x88	RW	Bit[7:0]: h_size_mipi[7:0]
P1:0x90	V_SIZE_MIPI_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: v_size_mipi[10:8]
P1:0x91	V_SIZE_MIPI_8LSB	0x40	RW	Bit[7:0]: v_size_mipi[7:0]
P1:0x92	HS_MODE_VF, HS_MODE, LP_CTL	0x02	RW	Bit[4]: hs_mode_vf 0: Clock switch per line 1: Clock switch per frame Bit[3]: hs_mode 0: Clock burst 1: Clock switch Bit[2:0]: lp_ctl
P1:0x93	R_CLK_POST	0x0E	RW	Bit[4:0]: r_clk_post
P1:0x94	R_LPC_CK, R_LPC_DAT	0x77	RW	Bit[7:4]: r_lpx_ck Bit[3:0]: r_lpx_dat
P1:0x95	R_CLK_PREPARE, R_HS_PREPARE	0x56	RW	Bit[7:4]: r_clk_prepare Bit[3:0]: r_hs_prepare
P1:0x96	R_HS_ZERO	0x1A	RW	Bit[4:0]: r_hs_zero
P1:0x97	DATA_ID	0x2B	RW	Bit[7:0]: data_id 0x2A: 8-bit mode 0x2B: 10-bit mode HSIZE low 8-bit
P1:0x98	R_CLK_TRAIL, R_HS_TRAIL	0x78	RW	Bit[7:4]: r_clk_trail Bit[3:0]: r_hs_trail
P1:0x9C	R_CLK_ZERO	0x22	RW	Bit[5:0]: r_clk_zero
P1:0xA1	MIPI_LS_START_NUM, TX_SPEED_AREA_SEL	0x03	RW	Bit[4:3]: mipi_ls_start_num Bit[2:0]: tx_speed_area_sel
P1:0xA2	R_INIT_M	0x0B	RW	Bit[7:0]: r_init[15:8]
P1:0xA3	R_INIT_L	0x40	RW	Bit[7:0]: r_init[7:0]

table 2-4 MIPI function related registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0xA4	R_EXIT, R_WAKEUP_MH	0x10	RW	Bit[5:2]: r_exit Bit[1:0]: r_wakeup[17:16]
P1:0xA5	R_WAKEUP_M	0x86	RW	Bit[7:0]: r_wakeup[15:8]
P1:0xA6	R_WAKEUP_L	0x88	RW	Bit[7:0]: r_wakeup[7:0]
P1:0xA7	DC_TEST_LP_LK	0x3F	RW	Bit[7]: dc_test_hsdc_en Bit[6]: dc_test_hsdd_en Bit[5:4]: dc_test_lp_ck_en Bit[3:2]: dc_test_lp_d1_en Bit[1:0]: Reserved for data lane's zero time control
P1:0xA8	DC_TEST_DATA_HS	0xFF	RW	Bit[7:0]: dc_test_data_hs
P1:0xAE	FRAME_END_DLY_8LSB	0x65	RW	Bit[7:0]: frame_end_dly[7:0]
P1:0xAF	FRAME_END_DLY_8MSB	0x01	RW	Bit[7:0]: frame_end_dly[15:8]
P1:0xB1	MIPI_EN, SHUTDOWNA	0x00	RW	Bit[1]: mipi_en Bit[0]: Shutdowna
P1:0xB2	MIPI_HSYNC_NUM	0x96	RW	Bit[7:0]: mipi_hsync_num Used in line sync mode
P1:0xB6	LS_MODE, LP_SST_EN	0x00	RW	Bit[4]: ls_mode Line sync mode enable Bit[3]: lp_sst_en

2.6.2 D_PHY related register configuration

table 2-5 D_PHY related registers

address	register name	default value	R/W	description
P0:0x44	MP_DA_SSEL, MP_CLK_SSEL, MP_PHASE_INV, MP_PHASE	0x05	RW	Bit[6]: mp_da_ssel Bit[5]: mp_clk_ssel Bit[4]: mp_phase_inv DPHY DDR clock phase inverted Bit[3:0]: mp_phase
P1:0x9D	HS_LEV	0x15	RW	Bit[6:0]: hs_lev Adjust high speed output difference mode voltage range and HS maximum value
P1:0x9E	HS_DRV	0x55	RW	Bit[7:0]: hs_drv

2.7 reset

The whole chip will be reset during power up. Manually applying a hard reset (RSTN = 0) upon power-up is recommended even through an on-chip power on reset is included. The hard reset (RSTN) is active low with an asynchronous design. The reset pulse width should be no less than 2 ms.

2.7.1 power on reset generation

The OS02G10 includes a RSTN pin that forces a complete hardware reset when it is pulled low (GND). Additionally, a power on reset (POR) is generated after core power becomes stable. The OS02G10 clears all registers to their default values.

2.7.2 software reset

A reset can also be initiated via the SCCB interface by writing P0:0x20 = 0x00. Then, all registers will be reset to their default values.

2.8 system clock control

2.8.1 MPLL (MIPI_PLL)

PLL1 generates a default 84 MHz pixel clock and an 840 MHz MIPI serial clock from a 10~36 MHz input clock. The VCO range is from 400 MHz to 940 MHz. A programmable clock divider is provided to generate different frequencies.

2.8.2 clock configuration

table 2-6 clock configuration related registers (sheet 1 of 2)

address	register name	default value	R/W	description
P0:0x2F	MPLL_MC	0x01	RW	Bit[7:0]: mpll_mc PLL output = [PLL input * (2- mpll_nc[7]) (mpll_nc[6:0]+3)/(mpll_mc+1)] Note: Parameters of registers will be enabled in next frame.
P0:0x30	DPLL_CP_DIV, PLL_DACCLK_DIV, MPLL_DIV	0x02	RW	Bit[5:4]: dpll_cp_div Bit[3:2]: dpll_dacclk_div Bit[1:0]: mpll_div

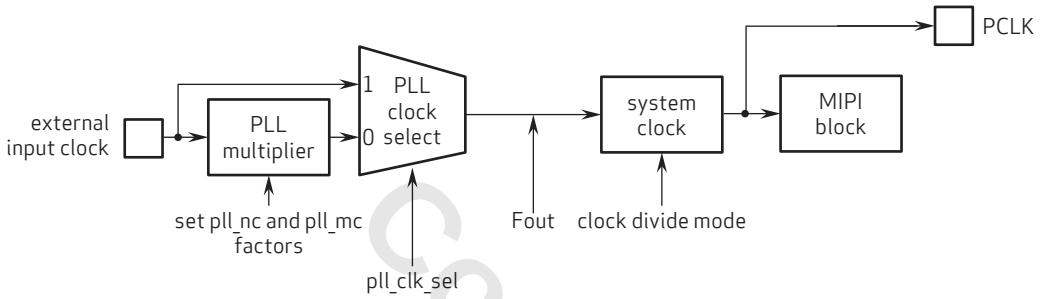
table 2-6 clock configuration related registers (sheet 2 of 2)

address	register name	default value	R/W	description
P0:0x31	CLK_MODE_BUF	0x11	RW	Bit[7]: pclk_ctrl 0: PCLK = pll_clk 1: PCLK = 1/2 pll_clk Bit[4]: row_clk_ctrl 0: row_clk = timer_clk 1: row_clk = 1/2 timer_clk Bit[0]: timer_clk_ctrl 0: timer_clk = pll_clk 1: timer_clk = 1/2 pll_clk Note: Parameters of registers will be enabled in next frame.
P0:0x38	PCLK_GATE_EN, PLL_GATE_EN	0x01	RW	Bit[4]: pclk_gate_en Pad PCLK gating enable signal 0: Disable PCLK gating 1: Enable PCLK gating Bit[0]: pll_gate_en PLL gating enable signal 0: Enable PLL gating 1: Disable PLL gating
P0:0x43	MP_RAW_SEL, MP_DOUBLE	0x01	RW	Bit[2:1]: mp_raw_sel MIPI RAW select 00: RAW10 /10 01: RAW8 /8 10: RAW12 /12 11: Disable timer_clk output Bit[0]: mp_double
P0:0x45	DPLL_SEL	0x00	RW	Bit[0]: dpll_sel Bypass loop for DAC clock

2.8.3 PLL clock scheme

The OS02G10 contains a phase locked loop (PLL) block, which generates all the necessary internal clocks from an external clock input. The internal function blocks of the PLL are shown in **figure 2-4**.

figure 2-4 PLL internal function block diagram



note

$$F_{out} = Fin * \frac{(2 - mpll\_mc[7]) \times (mpll\_nc[6:0] + 3)}{(mpll\_mc[2:0] + 1)}$$ is in range of 400 MHz to 940 MHz

2.9 power management

In power down mode, all internal clocks are stopped and all sensor modules are powered off. The register values will all be reset in power down mode.

In soft reset mode, all register values will be reset, but all internal clocks are kept and all sensor modules work normally.

In low power wake mode, all internal clocks are stopped and all sensor modules are powered off. The register values will all be kept in low power wake mode.

2.10 data lane parameters

The D-PHY converts parallel data from CSI_TOP to serial data that is compatible with MIPI protocol. Detailed time sequences are shown in **figure 2-5** and **figure 2-6**.

figure 2-5 high-speed data transmission bursts

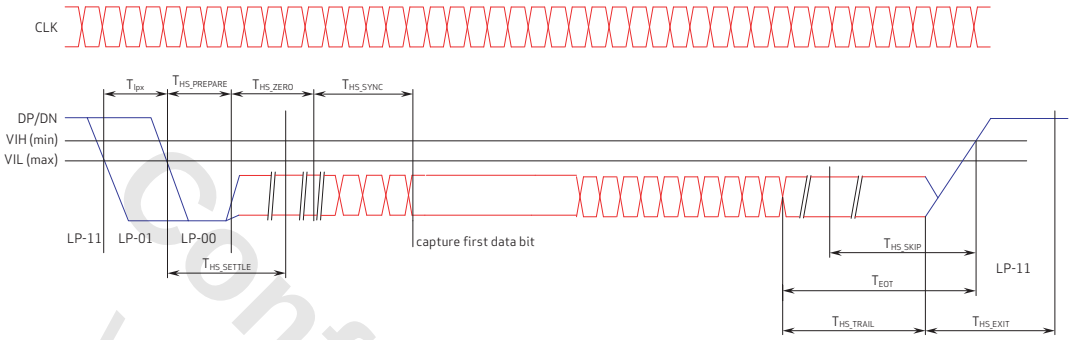


figure 2-6 switching the clock lane between clock transmission and low-power mode

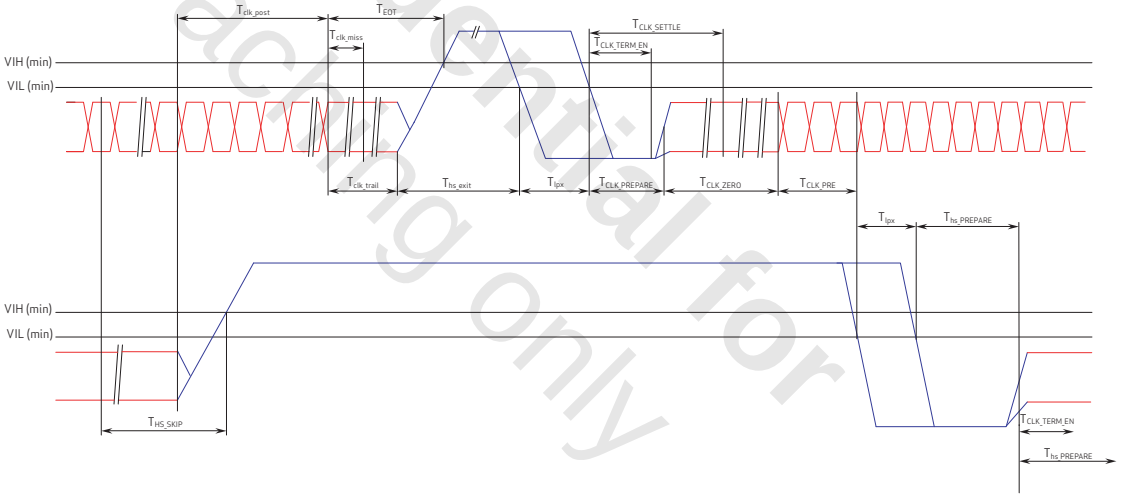


table 2-7 data lane parameters

parameter	target	min	max
$T_{HS-PREPARE}$	time that transmitter drives data lane LP-00 line state immediately before HS-0 Line state starts HS transmission	40 ns + 4*UI	85 ns + 6*UI
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that transmitter drives HS-0 state prior to transmitting sync sequence	145 ns + 10*UI	
$T_{HS-SETTLE}$	time interval which HS receive shall ignore any data lane HS transitions, starting from beginning of $T_{HS-PREPARE}$	85 ns + 6*UI	145 ns + 10*UI
$T_{HS-SKIP}$	time interval which HS-RX should ignore any transitions on data lane, following a HS burst end point of interval is defined as beginning of LP-11 state following HS burst	40 ns	55 ns + 4*UI
$T_{HS-TRAIL}$	time that transmitter drives HS-0 state after last payload clock bit of a HS transmission burst	max (n*8*UI, 60 ns + n*4*UI)	
T_{LPX}	transmitted length of any low-power state period	50 ns	
T_{WAKEUP}	time that a transmitter drives a Mark-1 state prior to a stop state in order to initiate an exit from ULPS	1 ms	

2.11 clock lane parameters

table 2-8 clock lane parameters

parameter	target	min	max
$T_{CLK-MISS}$	timeout for receiver to detect absence of clock transmission and disable clock lane HS-RX	60 ns	
$T_{CLK-POST}$	time that transmitter continues to send HS clock after last associated data lane has transitioned to LP mode interval is defined as period from end of $T_{HS-TRAIL}$ to beginning $T_{CLK-TRAIL}$	60 ns + 52*UI	
$T_{CLK-PRE}$	time that HS clock will be driven by transmitter prior to any associated data lane beginning transition from LP to HS mode	8*UI	
$T_{CLK-PREPARE}$	time that transmitter drives clock lane LP-00 line state immediately before HS-0 line state starts HS transmission	38 ns	95 ns
$T_{CLK-SETTLE}$	time interval which HS receive will ignore any clock lane HS transmissions, starting from beginning of $T_{CLK-PREPARE}$	95 ns	300 ns
$T_{CLK-TRAIL}$	time that transmitter drives HS-0 state after last payload clock bit of a HS transmission burst	60 ns	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that transmitter drives HS-0 state prior to starting clock	300 ns	
T_{EOT}	transmitted time interval from start of $T_{CLK-TRAIL}$ or $T_{HS-TRAIL}$, to start of LP-11 state following a HS burst		105 ns + n*12*UI

2.12 power up/off sequence

2.12.1 power up sequence

figure 2-7 power up sequence diagram

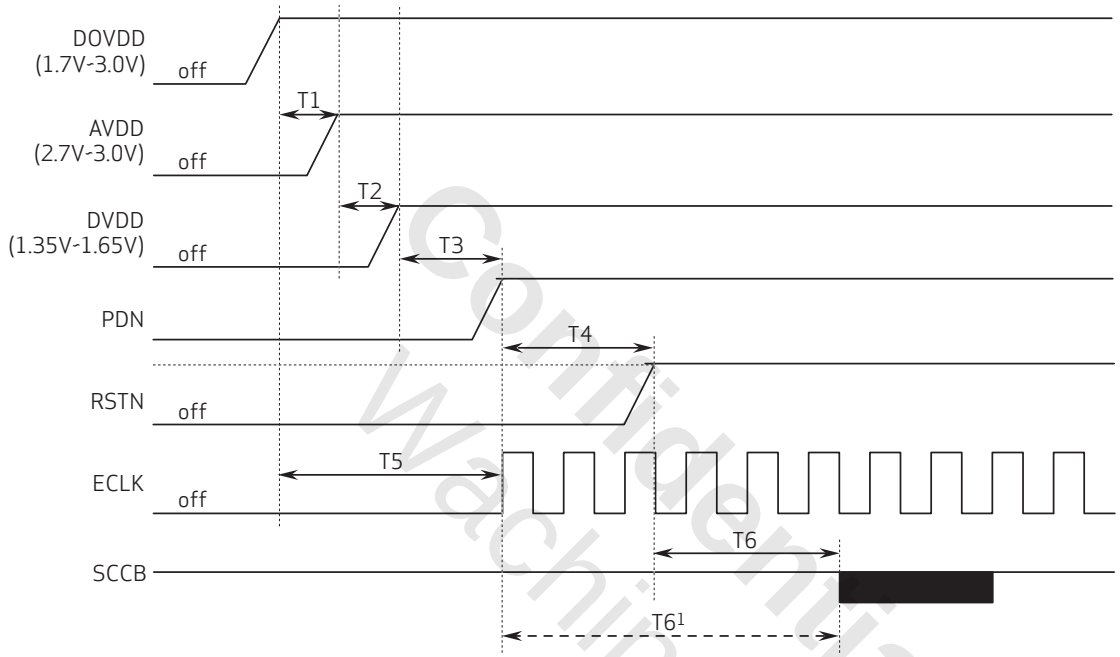


table 2-9 power up sequence parameters

symbol	description	min	unit
T1	delay from DOVDD to AVDD	0	ms
T2	delay from AVDD to DVDD	0	ms
T3	delay from DVDD stable to sensor power up stable	5	ms
T4	delay from sensor power up stable to RSTN pull up	4	ms
T5	delay from DOVDD stable to ECLK on	0	ms
T6	delay from sensor power up stable to SCCB initialization	5	ms
T6[1]	RSTN signal remains high at any time T6[1] = T4 + T6, T6[1] starts at sensor power up stable	9	ms

2.12.2 power off sequence

figure 2-8 power off sequence diagram

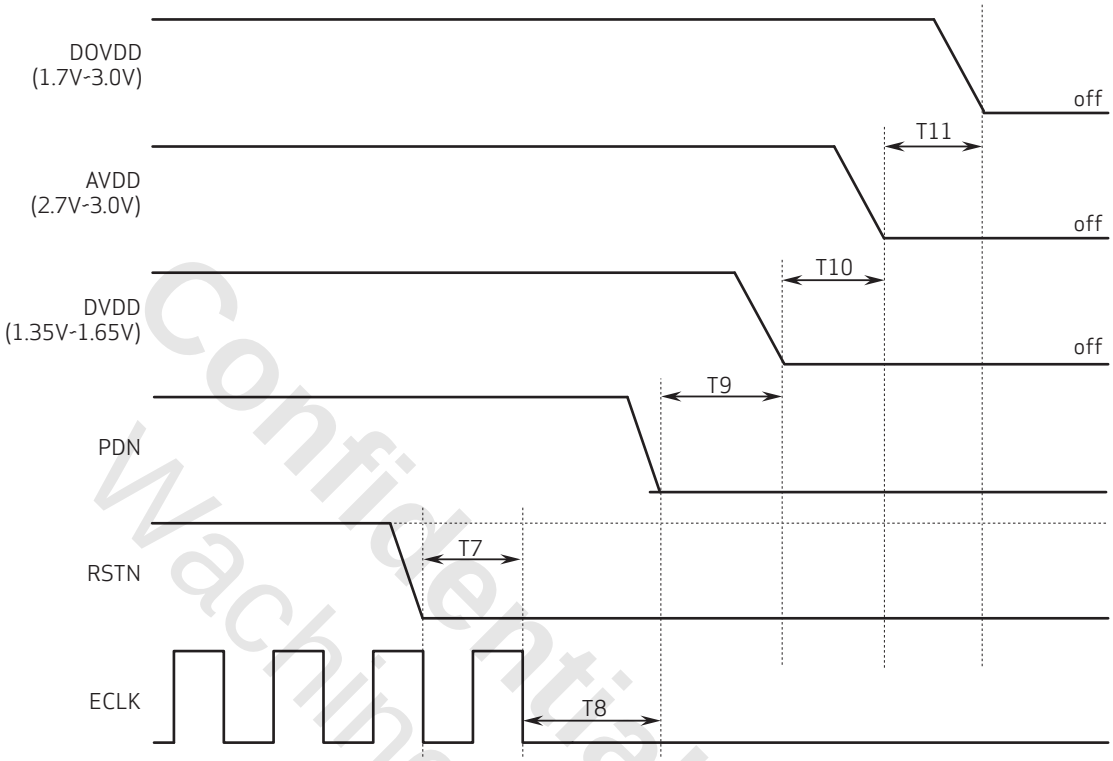


table 2-10 power off sequence parameters

symbol	description	min	unit
T7	delay from RSTN pull low stable to ECLK off	0	ms
T8	delay from ECLK off to sensor power down	0	ms
T9	delay from sensor power down to DVDD off	0	ms
T10	delay from DVDD off to AVDD off	0	ms
T11	delay from AVDD off to DOVDD off	0	ms

2.13 SCCB bus

2.13.1 single read and single write

The OS02G10 SCCB write address and read address can be selected by the SID pin. When the pin is set high, the write address is 0x7A and the read address is 0x7B. When the pin is set low, the write address is 0x78 and the read address is 0x79.

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First, the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

figure 2-9 illustrates the OS02G10 single read sequence and single write sequence.

figure 2-9 SCCB read and write message description (SID pin set high)

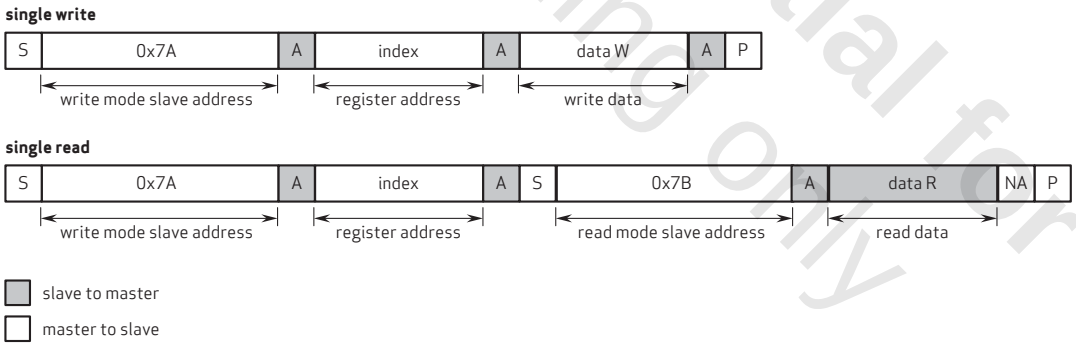
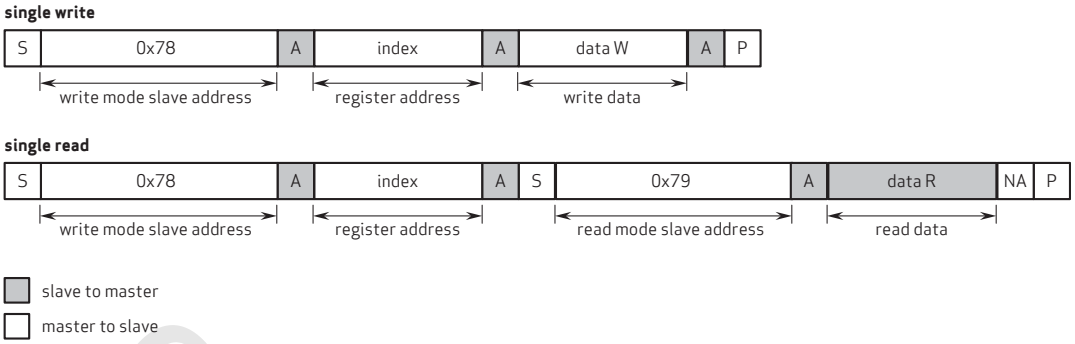


figure 2-10 SCCB read and write message description (SID pin set low)



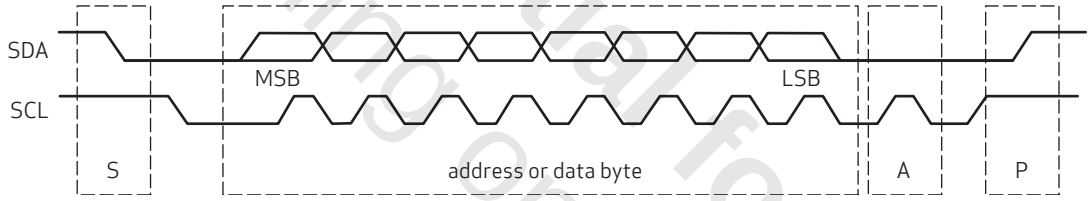
2.13.2 data bit transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the high period of the serial clock. It can only change when the serial clock is low. Data is transferred 8 bits at a time, followed by an acknowledge bit.

2.13.3 acknowledge bit

The OS02G10 will hold the value of the SDA pin to logic '0' during the logic '1' state of the acknowledge clock pulse on SCL.

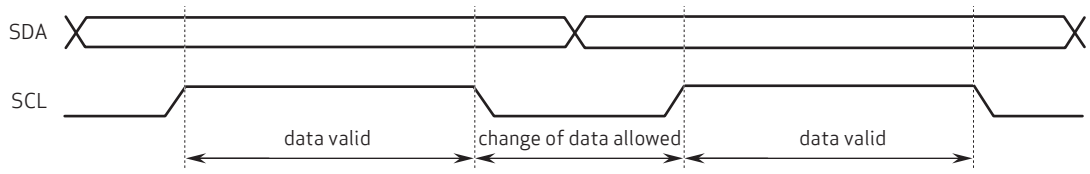
figure 2-11 SCCB acknowledge bit diagram



2.13.4 data valid

The master must ensure that the data is stable during the logic 1 state of the SCL pin. All transitions on the SDA pin can only occur when the logic level on the SCL pin is '0'.

figure 2-12 SCCB data transport diagram



2.13.5 timing parameter

figure 2-13 SCCB bus timing parameter diagram

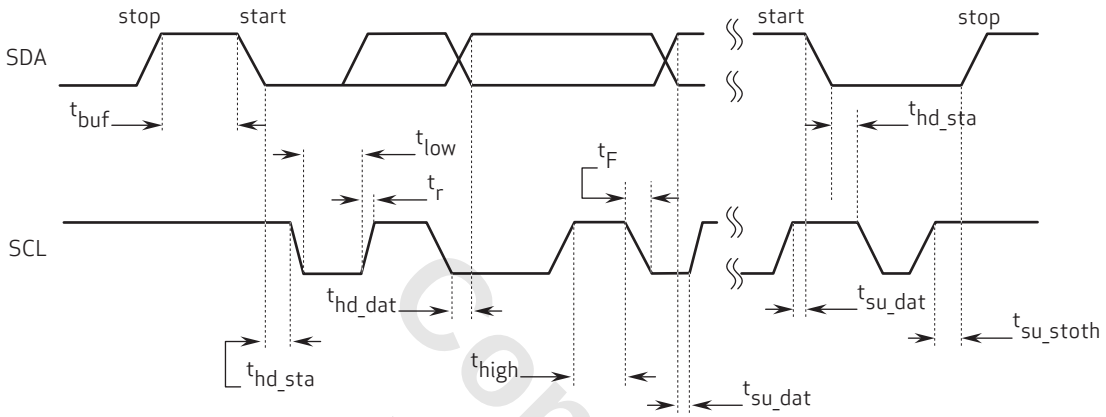


table 2-11 SCCB interface timing specifications

symbol	parameter	min	max	unit
f_{scl}	SCL clock frequency	–	400	kHz
t_{buf}	bus free time between a stop and a start	1.3	–	µs
t_{hd_sta}	hold time for a repeated start	0.6	–	µs
t_{low}	low period of SCL	1.3	–	µs
t_{high}	high period of SCL	0.6	–	µs
t_{su_sta}	setup time for a repeated start	0.6	–	µs
t_{hd_dat}	data hold time	0	–	µs
t_{su_dat}	data setup time	0.1	–	µs
t_r	rise time of SCL, SDA	–	0.3	µs
t_f	fall time of SCL, SDA	–	0.1	µs
t_{su_sto}	setup time for a stop	0.6	–	µs
t_{aa}	SCL low to data out valid	0.3	–	µs
t_{dh}	data out hold time	0.2	–	µs
C_b	capacitive load of bus line (SCL, SDA)	–	–	pf

3 block level description

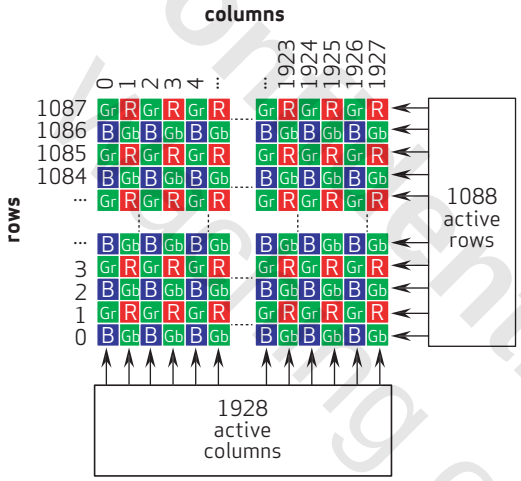
3.1 pixel array structure

The OS02G10 sensor has an image array of 1928 columns by 1088 rows (2,097,664 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color GR/BG array is arranged in line-alternating fashion. Of the 2,162,944 pixels, 2,073,600 (1920x1080) are active pixels and can be output.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



3.2 binning

The OS02G10 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode on, the voltage levels of adjacent pixels (of the same color) are averaged. The OS02G10 supports 2x2 binning, which is illustrated in **figure 3-2**, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged.

figure 3-2 example of 2x2 binning

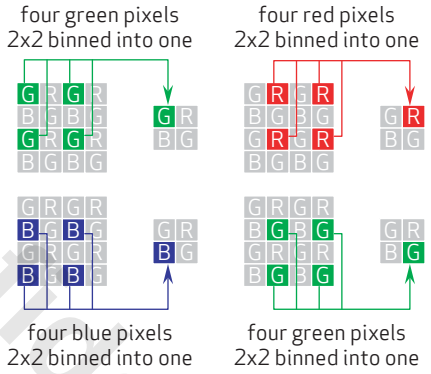


table 3-1 binning-related register

address	register name	default value	R/W	description
P1:0x31	COMM_CTRL	0x00	RW	Bit[4]: bypass_dsp Bit[3]: binning_en Bit[2]: v_binning_en Bit[1]: mode_720p Bit[0]: ana_window_en

4 image sensor core digital functions

4.1 mirror and flip

The OS02G10 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
P1:0x3F	FLIP/MIRROR	0x00	RW	Bit[1:0]: Flip/mirror 00: Normal 01: Mirror 10: Flip 11: Mirror and flip

4.2 windowing

The embedded windowing function extracts an image windowing area by defining four parameters, including horizontal start, horizontal width, vertical start, and vertical height. By properly setting the parameters, the portions within the sensor array size can be cropped as a visible area. The windowing function will not conflict with the mirror and flip function as shown in **figure 4-2**.

figure 4-2 windowing diagram

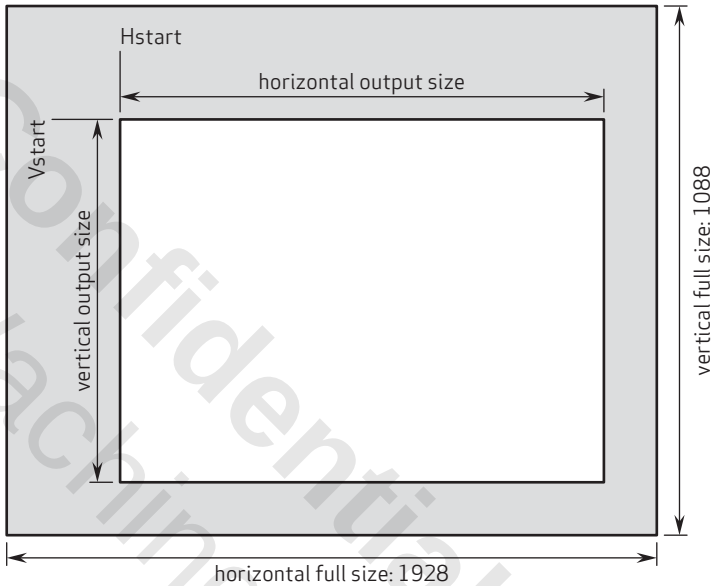


table 4-2 windowing control registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0x34	COL_ANA_ADDR_ START_2MSB, COL_ANA_ADDR_ SIZE_2MSB	0x00	RW	Bit[5:4]: Col_ana_addr_ size _2msb Bit[3:2]: Not used Bit[1:0]: Col_ana_addr_ start _2msb
P1:0x35	COL_ANA_ADDR_ START_8LSB	0x00	RW	Bit[7:0]: Col_ana_addr_start_ 8lsb
P1:0x36	COL_ANA_ADDR_ SIZE_8LSB	0x03	RW	Bit[7:0]: Col_ana_addr_ size _8lsb
P1:0x4A	VSTART_3MSB	0x00	RW	Bit[2:0]: VSTART[10:8]
P1:0x4B	VSTART_8LSB	0x00	RW	Bit[7:0]: VSTART[7:0]

table 4-2 windowing control registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0x4C	VSIZE_3MSB	0x04	RW	Bit[2:0]: VSIZE[10:8]
P1:0x4D	VSIZE_8LSB	0x40	RW	Bit[7:0]: VSIZE[7:0]

4.3 test pattern

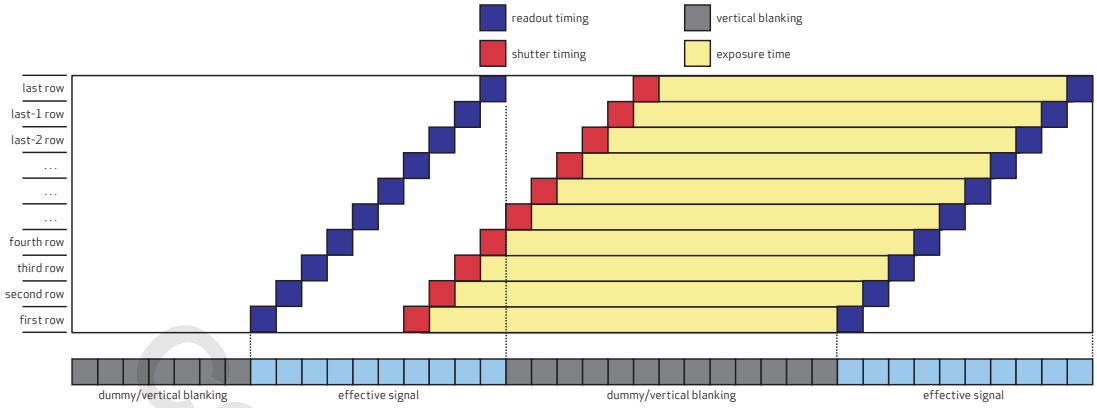
Test pattern and color bar are offered for testing purposes.

figure 4-3 test pattern diagram

4.4 shutter and integration time settings and continuous exposure control

The OS02G10 has a variable electronic shutter function that can control the integration time in row units. In addition, the OS02G10 performs rolling shutter operation in which electronic shutter and readout are performed sequentially for each row.

figure 4-4 shutter and integration time settings and continuous exposure control



The integration time can be controlled by varying the electronic shutter time. In the electronic shutter setting, the integration time is controlled by the EXP register ({P1:0x03, P1:0x04}).

4.4.1 exposure/gain control

The OS02G10 exposure registers are P1:0x03 and P1:0x04. The unit is Tline. Minimum exposure is 4 Tline. The maximum exposure is VTS-8. If the exposure is longer than VTS-8, the OS02G10 will automatically prolong the current VTS. To disable the VTS auto prolong feature, enable P1:0x0D[4] for manual VTS.

After registers P1:0x03 and P1:0x04 are set, register P1:0x01 must be set to 0x01 to trigger the new exposure.

The OS02G10 supports AGC gain. The AGC gain register is P1:0x24, 0x10 is 1x. Maximum AGC gain is 0xF8 = 15.5x. The AGC gain also needs register P1:0x01 to be set to 0x01 to trigger it.

The OS02G10 supports digital gain. The digital gain registers are P1:0x37 and P1:0x39. P1:0x39 = 0x40 is 1x digital gain. Maximum digital gain is (P1:0x37 = 0x07, P1:0x39 = 0xFF) = 32x. The minimum step is 1/64. The digital gain also needs register P1:0x01 to be set to 0x01 to trigger it. An example setting for exposure/AGC gain/digital gain control is shown below:

```
78 FD 01

78 03 01

78 04 54      ;exposure time 0x154

78 24 80      ;AGC gain 8x

78 39 80      ;digital gain 2x

78 01 01      ;trigger the new exposure/gain
```

The new exposure/AGC gain/digital gain will be valid after next frame.

4.4.2 HTS/VTS

The HTS/VTS registers are read only registers. Registers P1:0x41 and P1:0x42 are HTS registers. The unit is timer_clk. Registers P1:0x4E and P1:0x4F are VTS registers. The unit is Tline. To modify VTS, insert dummy lines with registers

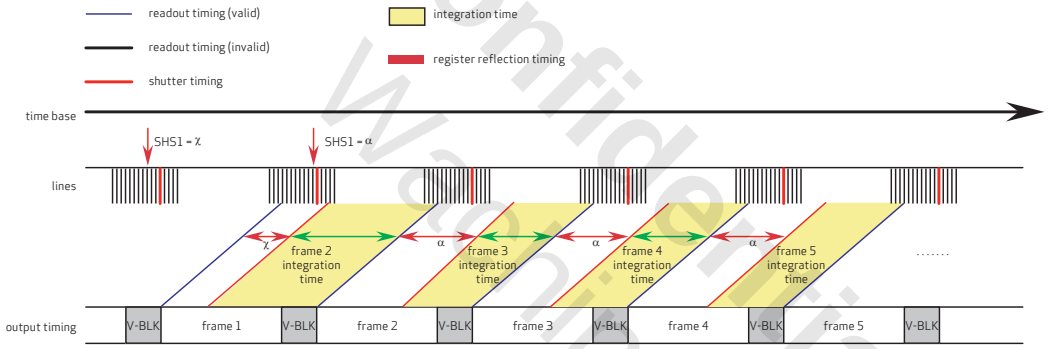
P1:0x05 and P1:0x06. Register P1:0x01 must be set to 0x01 to trigger the new Vblank. Registers P1:0x05 and P1:0x06 are Vblank registers. Registers P1:0x09 and P1:0x0A are Hblank registers.

For example, if the current dummy line is 1 line (P1:0x05 = 0x00 and P1:0x06 = 0x01) and the user wants to insert 16 dummy lines, the following setting is recommended:

```
78 FD 01
78 05 00
78 06 11       ;new dummy line
78 01 01
```

It is not recommended to change the HTS. If a change to the HTS is desired, please contact the local OmniVision FAE for support.

figure 4-5 integration time control within a frame



4.5 FSIN

Data output of the OS02G10 can be synchronized. The OS02G10 can be either a master or slave device in FSIN mode. After synchronization, the time difference between the data output of master and slave is less than 1H.

4.5.1 FSIN common control

table 4-3 FSIN control registers

address	register name	default value	R/W	description
P0:0x40	EXT_SYNC_MST_EN, EXT_SYNC_EN	0x00	RW	Bit[1]: ext_sync_mst_en Enable master mode of external sync function 0: OS02G10 is slave of external sync 1: OS02G10 is master of external sync Bit[0]: ext_sync_en Enable signal of external sync function 0: Disable external sync 1: Enable external sync
P1:0x0B	EXTER_SYNC_CTL	0x00	RW	Bit[7]: exter_sync_inv Bit[6]: exter_frame_num_x256_en When enabled, 1 LSB of exter_sync_frame_num (P1:0x17) equals 256 frames 0: Disable 1: Enable Bit[5]: exter_del_en 0: Disable 1: Enable Bit[4]: exter_sync_manual_en Configure a posedge in this bit to trigger a sync output in master mode Bit[3]: exter_sync_auto_en Sensor in master mode will send sync signal every exter_sync_frame_num (P1:0x17) frames automatically 0: Disable 1: Enable Bit[2]: sync_no_wait_en Bit[1]: External sync slave mode Bit[0]: External sync master mode 0: Disable 1: Enable
P1:0x15	EXP_SYNC_FRAME_NUM	0x0A	RW	Bit[7:0]: Interval frame number of auto external frame synchronize pulse

The master/slave mode, IE, OE, input polarity, output polarity, and input filter settings are programmed by register P0:0x1B.

4.6 auto black level calibration (ABLC)

The OS02G10 pixel array contains eight shielded (optical black) rows, among which 8/4 rows are used for black level calibration automatically. The whole ABLC process consists of three stages: black level obtained by averaging optical black rows, black level taking effect by triggers, and black level calibration.

4.6.1 obtaining black level

Several functions can be tuned during the process of obtaining black level.

The effective black level and current frame black level values can be read out by register. The readout data contains four decimals. Without trigger mode, the following data can be still read out.

Offset is a signed number, the range is -256~255.

table 4-4 BLC registers

address	register name	default value	R/W	description
P1:0xDD	BLC_BLACK_LEVEL_GB_8MSB	–	R	Bit[7:0]: black_level_gb[15:8] Effective Gb black level MSB
P1:0xDE	BLC_BLACK_LEVEL_B_8MSB	–	R	Bit[7:0]: black_level_b[15:8] Effective B black level MSB
P1:0xDF	BLC_BLACK_LEVEL_R_8MSB	–	R	Bit[7:0]: black_level_r[15:8] Effective R black level MSB
P1:0xE0	BLC_BLACK_LEVEL_GR_8MSB	–	R	Bit[7:0]: black_level_gr[15:8] Effective Gr black level MSB
P1:0xE1	BLC_BLACK_LEVEL_GB_8LSB	–	R	Bit[7:0]: black_level_gb[7:0] Effective Gb black level LSB
P1:0xE2	BLC_BLACK_LEVEL_B_8LSB	–	R	Bit[7:0]: black_level_b[7:0] Effective B black level LSB
P1:0xE3	BLC_BLACK_LEVEL_R_8LSB	–	R	Bit[7:0]: black_level_r[7:0] Effective R black level LSB
P1:0xE4	BLC_BLACK_LEVEL_GR_8LSB	–	R	Bit[7:0]: black_level_gr[7:0] Effective Gr black level LSB

4.6.2 trigger mode

Black level statistics are always calculated in real time. The OS02G10 supports the following trigger modes:

table 4-5 BLC statistics register

address	register name	default value	R/W	description
P1:0xFA	ABL_TRIGGER	0x00	RW	Bit[7]: Manual function Use with bit[0] at same time Bit[5]: Auto BLC enable Bit[4]: RPC function Bit[3]: Exp function Bit[2]: Mean function Bit[1]: frame_count reset Bit[0]: Manual function

Offset is a signed number, the range is -256~255.

table 4-6 BLC offset registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0xF0	GB_SUBOFFSET	0x00	RW	Bit[7:0]: Blacklevel offset, Gb channel, low 8 bits Total register is 9 bits with MSB at P1:0xF8[7] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF1	BLUE_SUBOFFSET	0x00	RW	Bit[7:0]: Blacklevel offset, blue channel, low 8 bits Total register is 9 bits with MSB at P1:0xF8[6] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF2	RED_SUBOFFSET	0x00	RW	Bit[7:0]: Blacklevel offset, red channel, low 8 bits Total register is 9 bits with MSB at P1:0xF8[5] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF3	GR_SUBOFFSET	0x00	RW	Bit[7:0]: Blacklevel offset, Gr channel, low 8 bits Total register is 9 bits with MSB at P1:0xF8[4] (-256~255, 0x100~0x0FF) Highest bit is sign bit

table 4-6 BLC offset registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0xF8	BLC_GB_SUBOFFSET, BLC_BLUE_SUBOFFSET, BLC_RED_SUBOFFSET, BLC_GR_SUBOFFSET	0x00	RW	Bit[7]: gb_suboffset[8] Bit[6]: blue_suboffset[8] Bit[5]: red_suboffset[8] Bit[4]: gr_suboffset[8]

4.7 one-time programmable (OTP) memory

The OS02G10 supports a maximum of 32 bytes of one-time programmable (OTP) memory. The first nine bytes of OTP memory are used to store chip identification and manufacturing information. The remaining 23 bytes are available for customization. There are two programming modes for the OTP.

4.7.1 batch mode

Before programming OTP data, the OTP_PGM_EN register must be set to 1'b1. Then, all written data needs to be configured by the OTP_DATA[31:0] register. Make sure the status register is 3'b000. Finally, begin writing the start register and begin programming. **table 4-7** shows the applicable registers.

table 4-7 OTP batch mode registers

address	register name	default value	R/W	description
P6:0x00~ P6:0x1F	OTP_DATA	0x00	RW	If OTP_PGM_EN = 1'b1: Program OTP Address0 Data If OTP_PGM_EN = 1'b0: Read OTP Address0 Data (read only)
P6:0x20	OTP_EF_PGM_STATE	–	R	OTP Program State
P6:0x21	OTP_ PGM_EN	0x00	RW	OTP Program and Read Mode Select 0: Read mode 1: Program mode
P6:0x2E	OTP_ PGM_START	0x00	RW	OTP Program Start Bit[3]: Program batch start Bit[2]: Program chip batch start (only address[8:0]) Bit[1]: Program user batch start (only address[31:9]) Bit[0]: Single program start
P6:0xFD	PAGE_FLAG	–	R	OTP Page Flag

4.7.2 single mode

The OTP_PGM_EN register must be set to 1'b1. Then, write to the OTP_PGM_ADDRESS and OTP_PGM_DATA registers. Make sure the status register is 3'b000. Finally, begin writing the start register and begin programming.

table 4-8 OTP single mode registers

address	register name	default value	R/W	description
P6:0x20	OTP_EF_PGM_STATE	–	R	OTP Program State
P6:0x21	OTP_ PGM_EN	0x00	RW	OTP Program and Read Mode Select 0: Read mode 1: Program mode
P6:0x22	OTP_ PGM_ADDRESS	0x11	RW	OTP Single Mode Program Address
P6:0x23	OTP_ PGM_DATA	0x00	RW	OTP Single Mode Program Data
P6:0x2E	OTP_ PGM_START	0x00	RW	OTP Program Start Bit[3]: Program batch start Bit[2]: Program chip batch start (only address[8:0]) Bit[1]: Program user batch start (only address[31:9]) Bit[0]: Single program start

When reading OTP data, the OTP_PGM_EN register must be set to 1'b0 and the data will be read out from the OTP_DATA[31:0] register after chip reset. The data can be manual controlled to load if the OTP_READ_LOAD register is configured.

table 4-9 OTP read register

address	register name	default value	R/W	description
P6:0x2F	OTP_ READ_LOAD	0x00	RW	OTP Load Data Enable

5 register tables

5.1 system [P0:0x02 - P0:0x51, P0:0xE7, P0:0xFD]

table 5-1 system registers (sheet 1 of 5)

address	register name	default value	R/W	description
P0:0x02	CHIP_ID	0x56	R	Bit[7:0]: chip_id
P0:0x03	CHIP_ID	0x02	R	Bit[7:0]: chip_id
P0:0x04	CHIP_ID	0x47	R	Bit[7:0]: chip_id
P0:0x05	CHIP_ID	0x00	R	Bit[7:0]: chip_id
P0:0x06~ P0:0x1A	RSVD	–	–	Reserved
P0:0x1B	PCLK_INV_BUF, EVSYNC_OE_BUF, EVSYNC_IE, OUT_END_BUF, OUT_ENS_BUF, OUT_ENP_BUF	0x37	RW	Bit[7:6]: Not used Bit[5]: pclk_inv_buf PCLK reverse enable 0: Disable PCLK reverse 1: Enable PCLK reverse Bit[4]: evsync_oe_buf Pad EVSYNC output enable signal 0: Enable output 1: Disable output Bit[3]: evsync_ie Pad EVSYNC IE enable signal 0: Enable output 1: Disable output Bit[2]: out_end_buf Pad DATAOUT[9:0] output enable signal 0: Enable output 1: Disable output Bit[1]: out_ens_buf Pads VSYNC and HSYNC output enable signal 0: Enable output 1: Disable output Bit[0]: out_enp_buf Pad PCLK output enable signal 0: Enable output 1: Disable output
P0:0x1C~ P0:0x1D	RSVD	–	–	Reserved

table 5-1 system registers (sheet 2 of 5)

address	register name	default value	R/W	description
P0:0x1E	DS_DATA, DS_PCLK, DS_HSYNC, DS_VSYNC	0x55	RW	Bit[7:6]: ds_vsync Driver current select signal of pad VSYNC Bit[5:4]: ds_hsync Driver current select signal of pad HSYNC Bit[3:2]: ds_pclk Driver current select signal of pad PCLK Bit[1:0]: ds_data Driver current select signal of pad DATAOUT[9:0]
P0:0x1F	RSVD	–	–	Reserved
P0:0x20	SOFT_RST	0x01	RW	Bit[7:1]: Not used Bit[0]: soft_rst Soft reset signal (cannot be self-cleared) 0: Enable soft reset 1: Disable soft reset
P0:0x21~ P0:0x2D	RSVD	–	–	Reserved
P0:0x2E	MPLL_NC	0x1B	RW	Bit[7:0]: mpll_nc
P0:0x2F	MPLL_MC	0x01	RW	Bit[7:0]: mpll_mc PLL output = [PLL input * (2 - mpll_nc[7]) (mpll_nc[6:0]+3)/(mpll_mc+1)] Note: Parameters of registers will be enabled in next frame.
P0:0x30	DPLL_CP_DIV, PLL_DACCLK_DIV, MPLL_DIV	0x02	RW	Bit[7:6]: Not used Bit[5:4]: dpll_cp_div Bit[3:2]: dpll_dacclk_div Bit[1:0]: mpll_div
P0:0x31	CLK_MODE_BUF	0x11	RW	Bit[7]: pclk_crtl 0: PCLK = pll_clk 1: PCLK = 1/2pll_clk Bit[6:5]: Not used Bit[4]: row_clk_ctrl 0: row_clk = timer_clk 1: row_clk = 1/2timer_clk Bit[3:1]: Not used Bit[0]: timer_clk_ctrl 0: timer_clk = pll_clk 1: timer_clk = 1/2pll_clk Note: Parameters of this register will be enabled in next frame.
P0:0x32	RSVD	–	–	Reserved

table 5-1 system registers (sheet 3 of 5)

address	register name	default value	R/W	description
P0:0x33	DPLL_BIAS	0x01	RW	Bit[7:3]: Not used Bit[2:0]: dpll_bias PLL chargepump current control
P0:0x34	RSVD	–	–	Reserved
P0:0x35	DPLL_DCTL, MPLL_BIAS, MPLL_DCTL	0x02	RW	Bit[7:5]: Not used Bit[4]: dpll_dctl Choose PLL's PFD delay time to remove dead zone Bit[3:1]: mpll_bias PLL chargepump current control Bit[0]: mpll_dctl Choose PLL's PFD delay time to remove dead zone
P0:0x36	PWD_PLL	0x00	RW	Bit[7:1]: Not used Bit[0]: pwd_pll Power down control of PLL 0: Disable power down of PLL 1: Enable power down of PLL
P0:0x37	PWD_ASP	0x00	RW	Bit[7:1]: Not used Bit[0]: pwd_asp Power down control of ASP 0: Disable power down of ASP 1: Enable power down of ASP
P0:0x38	PCLK_GATE_EN, PLL_GATE_EN	0x01	RW	Bit[7:5]: Not used Bit[4]: pclk_gate_en Pad PCLK gating enable signal 0: Disable PCLK gating 1: Enable PCLK gating Bit[3:1]: Not used Bit[0]: pll_gate_en PLL gating enable signal 0: Disable PLL gating 1: Enable PLL gating
P0:0x39~ P0:0x3F	RSVD	–	–	Reserved

table 5-1 system registers (sheet 4 of 5)

address	register name	default value	R/W	description
P0:0x40	EXT_SYNC_MST_EN, EXT_SYNC_EN	0x00	RW	Bit[7:2]: Not used Bit[1]: ext_sync_mst_en Enable master mode of external sync function 0: OS02G10 is slave of external sync 1: OS02G10 is master of external sync Bit[0]: ext_sync_en Enable signal of external sync function 0: Disable external sync 1: Enable external sync
P0:0x41	DPLL_NC	0x0B	RW	Bit[7:6]: Not used Bit[5:0]: dpll_nc
P0:0x42	DPLL_MC	0x3C	RW	Bit[7:2]: Not used Bit[1:0]: dpll_mc PLL output = [PLL input * (pll_nc+3) /(pll_mc+1)] Note: Parameters of this register will be enabled in next frame.
P0:0x43	MP_RAW_SEL, MP_DOUBLE	0x01	RW	Bit[7:3]: Not used Bit[2:1]: mp_raw_sel MIPI RAW select 00: RAW10 /10 01: RAW8 /8 10: RAW12 /12 11: Disable timer_clk output Bit[0]: mp_double
P0:0x44	MP_DA_SSEL, MP_CLK_SSEL, MP_PHASE_INV, MP_PHASE	0x05	RW	Bit[7]: Not used Bit[6]: mp_da_ssel Bit[5]: mp_clk_ssel Bit[4]: mp_phase_inv DPHY DDR clock phase inverted Bit[3:0]: mp_phase
P0:0x45	DPLL_SEL	0x00	RW	Bit[7:1]: Not used Bit[0]: dpll_sel Bypass loop for DAC clock
P0:0x46~ P0:0x4F	RSVD	–	–	Reserved
P0:0x50	I2C_DEV_ADDR_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: i2c_dev_addr_en i2c_dev_addr enable signal 0: Disable i2c_dev_addr 1: Enable i2c_dev_addr

table 5-1 system registers (sheet 5 of 5)

address	register name	default value	R/W	description
P0:0x51	I2C_DEV_ADDR	0x3D	RW	Bit[7]: Not used Bit[6:0]: i2c_dev_addr Manual I2C device address
P0:0xE7	REG_UPDATE_MODE, REG_UPDATE_CMD	0x00	RW	Bit[7:2]: Not used Bit[1]: reg_update_mode Bit[0]: reg_update_cmd
P0:0xFD	PAGE_FLG	0x00	RW	Bit[7:3]: Not used Bit[2:0]: page_flg

5.2 sensor_ctrl [P1:0x01 - P1:0x4F, P1:0x8E - P1:0xCB, P1:0xDD - P1:0xFB]

table 5-2 sensor_ctrl registers (sheet 1 of 9)

address	register name	default value	R/W	description
P1:0x01	EXP_RPC_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: exp_rpc_en Enable of frame sync signal 0: Disable 1: Enable
P1:0x02	RSVD	–	–	Reserved
P1:0x03	BUF_EXP_8MSB	0x00	RW	Bit[7:0]: buf_exp[15:8]
P1:0x04	BUF_EXP_8LSB	0x9A	RW	Bit[7:0]: buf_exp[7:0]
P1:0x05	VBLANK_BUF_8MSB	0x00	RW	Bit[7:0]: Vertical blank[15:8]
P1:0x06	VBLANK_BUF_8LSB	0x00	RW	Bit[7:0]: Vertical blank[7:0]
P1:0x07	RSVD	–	–	Reserved
P1:0x08	VPOS_BLANK	0x01	RW	Bit[7:4]: Not used Bit[3:0]: vpos_blank
P1:0x09	HBLANK_4MSB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Horizontal blank[11:8]
P1:0x0A	HBLANK_8LSB	0x00	RW	Bit[7:0]: Horizontal blank[7:0]

table 5-2 sensor_ctrl registers (sheet 2 of 9)

address	register name	default value	R/W	description
P1:0x0B	EXTER_SYNC_CTL	0x00	RW	External Frame Synchronize Control Signal Bit[7]: exter_sync_inv Bit[6]: exter_frame_num_x256_en When enabled, 1 LSB of exter_sync_frame_num (P1:0x17) equals 256 frames 0: Disable 1: Enable Bit[5]: exter_del_en 0: Disable 1: Enable Bit[4]: exter_sync_manual_en Configure a posedge in this bit to trigger a sync output in master mode Bit[3]: exter_sync_auto_en Sensor in master mode will send sync signal every exter_sync_frame_num (P1:0x17) frames automatically 0: Disable 1: Enable Bit[2]: sync_no_wait_en Bit[1]: External sync slave mode Bit[0]: External sync master mode 0: Disable 1: Enable
P1:0x0C	EXTER_SYNC_OUT_WIDTH	0x08	RW	Bit[7:0]: Width of sync signal output when sensor is configured as master and with cycle as a unit
P1:0x0D	FRAME_EXP_SEPARATE_EN, RPC_TEST, TIMING_TEST_EN, TEST_EN	0x00	RW	Bit[7:5]: Not used Bit[4]: frame_exp_separate_en Bit[3]: rpc_test Bit[2]: Not used Bit[1]: timing_test_en Bit[0]: test_en Test pattern test enable 0: Disable 1: Enable
P1:0x0E	FRAME_LENGTH_NUM_8MSB	0x04	RW	Bit[7:0]: frame_length[15:8]
P1:0x0F	FRAME_LENGTH_NUM_8LSB	0x50	RW	Bit[7:0]: frame_length[7:0]
P1:0x10	EXT_SYNC_TEST_RESULT, EXT_SYNC_TEST_DONE, EXT_SYNC_TEST_EN	0x00	RW	Bit[7:3]: Not used Bit[2]: ext_sync_test_result Bit[1]: ext_sync_test_done Bit[0]: ext_sync_test_en

table 5-2 sensor_ctrl registers (sheet 3 of 9)

address	register name	default value	R/W	description
P1:0x12~ P1:0x14	RSVD	–	–	Reserved
P1:0x15	EXP_SYNC_FRAME_ NUM	0x0A	RW	Bit[7:0]: Interval frame number of auto external frame synchronize pulse
P1:0x16	DEL_FRAME_NUM, SWITCH_DEL_FRAME_ EN, PWD_DEL_FRAME_ EN, MANUAL_DEL_ FRAME_EN, UPDOWN_DEL_ FRAME_EN, RST_DEL_EN, RST_COLROW_EN	0x00	RW	Bit[7:6]: del_frame_num Bit[5]: switch_del_frame_en Bit[4]: pwd_del_frame_en Bit[3]: manual_del_frame_en Bit[2]: updown_del_frame_en Bit[1]: rst_del_en Bit[0]: rst_colrow_en
P1:0x17~ P1:0x22	RSVD	–	–	Reserved
P1:0x23	RPC1	0x20	RW	Bit[7:0]: RPC1
P1:0x24	PGA_GAIN1_CTL	0x20	RW	Bit[7:0]: pga_gain1_ctl
P1:0x25~ P1:0x27	RSVD	–	–	Reserved
P1:0x28	ANA_V_DUMMY_SIZE	0x00	RW	Bit[7:0]: ana_v_dummy_size
P1:0x29	COL_TEST_RST	0x00	RW	Bit[7:1]: Not used Bit[0]: col_test_rst
P1:0x2A~ P1:0x2F	RSVD	–	–	Reserved
P1:0x30	SA_MODE, SA_IRST_CTL, SA_PW1_CTL	0x22	RW	Analog Internal Debug Register
P1:0x31	COMM_CTRL	0x00	RW	Bit[7:5]: Not used Bit[4]: bypass_dsp Bit[3]: binning_en Bit[2]: v_binning_en Bit[1]: mode_720p Bit[0]: ana_window_en
P1:0x32	QUICK_EXP_DEL	0x00	RW	Bit[7:1]: Not used Bit[0]: quick_exp_del
P1:0x33	RSVD	–	–	Reserved
P1:0x34	COL_ANA_ADDR_ START_2MSB, COL_ANA_ADDR_ SIZE_2MSB	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Col_ana_addr_ size _2msb Bit[3:2]: Not used Bit[1:0]: Col_ana_addr_ start _2msb

table 5-2 sensor_ctrl registers (sheet 4 of 9)

address	register name	default value	R/W	description
P1:0x35	COL_ANA_ADDR_ START_8LSB	0x00	RW	Bit[7:0]: Col_ana_addr_start_8lsb
P1:0x36	COL_ANA_ADDR_ SIZE_8LSB	0x03	RW	Bit[7:0]: Col_ana_addr_ size _8lsb
P1:0x37	DIG_GAIN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: dig_gain[10:8]
P1:0x38	RPC_31_SEL, PGA_GAIN1_MSB8	0x10	RW	Bit[7:5]: Not used Bit[4]: rpc_31_sel Bit[3:1]: Not used Bit[0]: pga_gain1[8]
P1:0x39	DIG_GAIN	0x40	RW	Bit[7:0]: Global digital gain (0x37:39, 1x~32x)[7:0] 0x040:1x 0x7FF:32x Accuracy is 1/64
P1:0x3A	VDELAY_BUF_8MSB	0x00	RW	Bit[7:0]: vdelay_buf[15:8]
P1:0x3B	VDELAY_BUF_8LSB	0x00	RW	Bit[7:0]: vdelay_buf[7:0]
P1:0x3C	ULP_PWD_A_EN, DUMMY_RST_ADDR_ GATING, DUMMY_ROW1	0x0A	RW	Bit[7]: p_pwd_a_en Bit[6]: dummy_rst_addr_gating Bit[5:0]: dummy_row1
P1:0x3D	RSVD	–	–	Reserved
P1:0x3E	EXTER_SYNC_DLY_ NUM	0x00	RW	Bit[7:0]: exter_sync_dly_num
P1:0x3F	FLIP/MIRROR	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Flip/mirror 00: Normal 01: Mirror 10: Flip 11: Mirror and flip
P1:0x40	RSVD	–	–	Reserved
P1:0x41	HS_PERIOD_NUM_ 5MSB	–	R	Bit[7:5]: Not used Bit[4:0]: hs_period_num[12:8]
P1:0x42	HS_PERIOD_NUM_ 8LSB	–	R	Bit[7:0]: hs_period_num[7:0]
P1:0x43~ P1:0x45	RSVD	–	–	Reserved
P1:0x46	DC_LEVEL_LIMIT_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Dc_level_limit_en
P1:0x47	DC_LEVEL_LIMIT	0x20	RW	Bit[7:0]: Limitation of DC

table 5-2 sensor_ctrl registers (sheet 5 of 9)

address	register name	default value	R/W	description
P1:0x48	BLC_DATA_LIMIT	0xE8	RW	Bit[7:0]: Limitation of data output
P1:0x49	BLC_DATA_LIMIT[13:12], DC_LEVEL_LIMIT[10:8]	0x33	RW	Bit[7:6]: Not used Bit[5:4]: Limitation of data output Bit[3]: Not used Bit[2:0]: Limitation of DC
P1:0x4A	VSTART_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: VSTART[10:8]
P1:0x4B	VSTART_8LSB	0x00	RW	Bit[7:0]: VSTART[7:0]
P1:0x4C	VSIZE_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: VSIZE[10:8]
P1:0x4D	VSIZE_8LSB	0x40	RW	Bit[7:0]: VSIZE[7:0]
P1:0x4E	FRAME_LENGTH_ READONLY_8MSB	–	R	Bit[7:0]: frame_length[15:8]
P1:0x4F	FRAME_LENGTH_ READONLY_8LSB	–	R	Bit[7:0]: frame_length[7:0]
P1:0x8E	H_SIZE_MIPI_4MSB	0x07	RW	Bit[7:4]: Not used Bit[3:0]: h_size_mipi[11:8]
P1:0x8F	H_SIZE_MIPI_8LSB	0x88	RW	Bit[7:0]: h_size_mipi[7:0]
P1:0x90	V_SIZE_MIPI_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: v_size_mipi[10:8]
P1:0x91	V_SIZE_MIPI_8LSB	0x40	RW	Bit[7:0]: v_size_mipi[7:0]
P1:0x92	HS_MODE_VF, HS_MODE, LP_CTL	0x02	RW	Bit[7:5]: Not used Bit[4]: hs_mode_vf 0: Clock switch per line 1: Clock switch per frame Bit[3]: hs_mode 0: Clock burst 1: Clock switch Bit[2:0]: lp_ctl
P1:0x93	R_CLK_POST	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: r_clk_post
P1:0x94	R_LPC_CK, R_LPC_DAT	0x77	RW	Bit[7:4]: r_lpc_ck Bit[3:0]: r_lpc_dat
P1:0x95	R_CLK_PREPARE, R_HS_PREPARE	0x56	RW	Bit[7:4]: r_clk_prepare Bit[3:0]: r_hs_prepare
P1:0x96	R_HS_ZERO	0x1A	RW	Bit[7:5]: Not used Bit[4:0]: r_hs_zero

table 5-2 sensor_ctrl registers (sheet 6 of 9)

address	register name	default value	R/W	description
P1:0x97	DATA_ID	0x2B	RW	Bit[7:0]: data_id 0x2A: 8-bit mode 0x2B: 10-bit mode HSIZE low 8-bit
P1:0x98	R_CLK_TRAIL, R_HS_TRAIL	0x78	RW	Bit[7:4]: r_clk_trail Bit[3:0]: r_hs_trail
P1:0x99~ P1:0x9B	RSVD	–	–	Reserved
P1:0x9C	R_CLK_ZERO	0x22	RW	Bit[7:6]: Not used Bit[5:0]: r_clk_zero
P1:0x9D	HS_LEV	0x15	RW	Bit[7]: Not used Bit[6:0]: hs_lev Adjust high speed output difference mode voltage range and HS maximum value
P1:0x9E	HS_DRV	0x55	RW	Bit[7:0]: hs_drv
P1:0x9F~ P1:0xA0	RSVD	–	–	Reserved
P1:0xA1	MIPI_LS_START_NUM, TX_SPEED_AREA_SEL	0x03	RW	Bit[7:5]: Not used Bit[4:3]: mipi_ls_start_num Bit[2:0]: tx_speed_area_sel
P1:0xA2	R_INIT_M	0x0B	RW	Bit[7:0]: r_init[15:8]
P1:0xA3	R_INIT_L	0x40	RW	Bit[7:0]: r_init[7:0]
P1:0xA4	R_EXIT, R_WAKEUP_MH	0x10	RW	Bit[7:6]: Not used Bit[5:2]: r_exit Bit[1:0]: r_warkup[17:16]
P1:0xA5	R_WAKEUP_M	0x86	RW	Bit[7:0]: r_wakeup[15:8]
P1:0xA6	R_WAKEUP_L	0x88	RW	Bit[7:0]: r_wakeup[7:0]
P1:0xA7	DC_TEST_LP_LK	0x3F	RW	Bit[7]: dc_test_hsdc_en Bit[6]: dc_test_hsdd_en Bit[5:4]: dc_test_lp_ck_en Bit[3:2]: dc_test_lp_d1_en Bit[1:0]: Reserved for data lane's zero time control
P1:0xA8	DC_TEST_DATA_HS	0xFF	RW	Bit[7:0]: dc_test_data_hs
P1:0xA9~ P1:0xAD	RSVD	–	–	Reserved
P1:0xAE	FRAME_END_DLY_8LSB	0x65	RW	Bit[7:0]: frame_end_dly[7:0]

table 5-2 sensor_ctrl registers (sheet 7 of 9)

address	register name	default value	R/W	description
P1:0xAF	FRAME_END_DLY_ 8MSB	0x01	RW	Bit[7:0]: frame_end_dly[15:8]
P1:0xB0	RSVD	–	–	Reserved
P1:0xB1	MIPI_EN, SHUTDOWNA	0x00	RW	Bit[7:2]: Not used Bit[1]: mipi_en Bit[0]: Shutdowna
P1:0xB2	MIPI_HSYNC_NUM	0x96	RW	Bit[7:0]: mipi_hsync_num Used in line sync mode
P1:0xB3~ P1:0xB5	RSVD	–	–	Reserved
P1:0xB6	PAUSE_CK, LS_MODE, LP_SST_EN, INIT, ULP_MODE, TESTMODE	0x00	RW	Bit[7:6]: Not used Bit[5]: pause_ck Bit[4]: ls_mode Line sync mode enable Bit[3]: lp_sst_en Bit[2]: Init Bit[1]: ulp_mode Bit[0]: Test mode
P1:0xB7~ P1:0xC9	RSVD	–	–	Reserved
P1:0xCA	TIMING_TEST_HSYNC_N UM	0xC4	RW	Bit[7:0]: timing_test_hsync_num[7:0]
P1:0xCB	TIMING_TEST_HSYNC_N UM	0x03	RW	Bit[7:3]: Not used Bit[2:0]: timing_test_hsync_num[10:8]
P1:0xDD	BLACK_LEVEL_GB_ MSB	–	R	Bit[7:0]: black_level_gb[15:8] Effective Gb black level MSB
P1:0xDE	BLACK_LEVEL_B_ MSB	–	R	Bit[7:0]: black_level_b[15:8] Effective B black level MSB
P1:0xDF	BLACK_LEVEL_R_ MSB	–	R	Bit[7:0]: black_level_r[15:8] Effective R black level MSB
P1:0xE0	BLACK_LEVEL_GR_ MSB	–	R	Bit[7:0]: black_level_gr[15:8] Effective Gr black level MSB
P1:0xE1	BLACK_LEVEL_GB_ 8LSB	–	R	Bit[7:0]: black_level_gb[7:0] Effective Gb black level LSB
P1:0xE2	BLACK_LEVEL_B_ 8LSB	–	R	Bit[7:0]: black_level_b[7:0] Effective B black level LSB
P1:0xE3	BLACK_LEVEL_R_ 8LSB	–	R	Bit[7:0]: black_level_r[7:0] Effective R black level LSB

table 5-2 sensor_ctrl registers (sheet 8 of 9)

address	register name	default value	R/W	description
P1:0xE4	BLACK_LEVEL_GR_ 8LSB	–	R	Bit[7:0]: black_level_gr[7:0] Effective Gr black level LSB
P1:0xE5	RPC1_TMP1	–	R	Bit[7:0]: rpc1_tmp1
P1:0xE6	RSVD	–	–	Reserved
P1:0xE7	REG_UPDATE_MODE, REG_UPDATE_CMD	0x00	RW	Bit[7:2]: Not used Bit[1]: reg_update_mode Bit[0]: reg_update_cmd
P1:0xE8~ P1:0xEF	RSVD	–	–	Reserved
P1:0xF0	GB_SUBOFFSET	0x00	RW	Bit[7:0]: Blacklevel offset, Gb channel, low 8 bits Total register is 9 bits with MSB at P1:0xF8[7] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF1	BLUE_SUBOFFSET	0x00	RW	Bit[7:0]: Blacklevel offset, blue channel, low 8 bits Total register is 9 bits with MSB at P1:0xF8[6] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF2	RED_SUBOFFSET	0x00	RW	Bit[7:0]: Blacklevel offset, red channel, low 8 bits Total register is 9 bits with MSB at P1:0xF8[5] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF3	GR_SUBOFFSET	0x00	RW	Bit[7:0]: Blacklevel offset, Gr channel, low 8 bits Total register is 9 bits with MSB at P1:0xF8[4] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF4~ P1:0xF7	RSVD	–	–	Reserved
P1:0xF8	BLC_GB_SUBOFFSET, BLC_BLUE_SUBOFFSET, BLC_RED_SUBOFFSET, BLC_GR_SUBOFFSET, BL_POSITION_SET2, BL_POSITION_SET	0x00	RW	Bit[7]: gb_suboffset[8] Bit[6]: blue_suboffset[8] Bit[5]: red_suboffset[8] Bit[4]: gr_suboffset[8] Bit[3:2]: bl_position_set2 Bit[1:0]: bl_position_set
P1:0xF9	RSVD	–	–	Reserved

table 5-2 sensor_ctrl registers (sheet 9 of 9)

address	register name	default value	R/W	description
P1:0xFA	ABL_TRIGGER	0x00	RW	Bit[7]: Manual function Use with bit[0] at same time Bit[6]: Not used Bit[5]: Auto BLC enable Bit[4]: RPC function Bit[3]: Exp function Bit[2]: Mean function Bit[1]: frame_count reset Bit[0]: Manual function
P1:0xFB	ABL	0x00	RW	Bit[7]: Not used Bit[6]: blc_test_en 0: Low 10 bits output mode 1: High 10 bits output mode Bit[5:4]: Not used Bit[3]: ob2_en Bit[2:1]: blc_en 00: 1 frame average mode 01: 4 frames average mode 10: 8 frames average mode 11: 1 frame average mode Bit[0]: blc_mode 0: Blacklevel disable 1: Blacklevel enable

5.3 ISP [P2:0x2F - P2:0x5F, P2:0xA0 - P2:0xA7, P2:0xF9 - P2:0xFA]

table 5-3 ISP registers (sheet 1 of 3)

address	register name	default value	R/W	description
P2:0x2F	FIX_STATE_EN, FIX_STATE_MODE	0x00	RW	Bit[7:5]: Reserved Bit[4]: fix_state_en Fixed state enable 0: Disable fixed state 1: Enable fixed state Bit[3:1]: Reserved Bit[0]: fix_state_mode Mode of fixed state
P2:0x30	EXP_HEQ_DUMMY _8HSM	0x04	RW	Bit[7:0]: exp_heq_dummy[15:8] Exposure threshold high 8 bits between normal and dummy

table 5-3 ISP registers (sheet 2 of 3)

address	register name	default value	R/W	description
P2:0x31	EXP_HEQ_DUMMY _8LSM	0x60	RW	Bit[7:0]: exp_heq_dummy[7:0] Exposure threshold low 8 bits between normal and dummy
P2:0x32	RPC_HEQ_DUMMY_ 8LSM	0x80	RW	Bit[7:0]: rpc_heq_dummy[7:0] RPC threshold low 8 bits between normal and dummy
P2:0x33	RPC_HEQ_DUMMY _MSB	0x00	RW	Bit[7:1]: Not used Bit[0]: rpc_heq_dummy[8] RPC threshold high 1 bit between normal and dummy
P2:0x34	DPC_EN	0xFE	RW	Bit[7]: dpc_en Bit[6:0]: Reserved
P2:0x35	BUF_OUTMODE1	0x00	RW	Bit[7:6]: Reserved Bit[5]: unpro_raw_out_en Bit[4:0]: Reserved
P2:0x36	BUF_OUTMODE2	0x00	RW	Bit[7:5]: Reserved Bit[4]: domu_en Bit[3]: VSYNC inversion Bit[2]: HSYNC inversion Bit[1:0]: Reserved
P2:0x37~ P2:0x5C	RSVD	–	–	Reserved
P2:0x5D	AWBGAIN_POSITION_SET, BAYER_ORDER	0x01	RW	Bit[7:5]: Reserved Bit[4]: awbgain_position_set Bit[3:2]: Reserved Bit[1:0]: bayer_order
P2:0x5E	SIF_EN, FIRST_CHANNEL_EN, AUTO_FIRST_EN, BR_FIRST	0x02	RW	Bit[7:6]: Not used Bit[5]: sif_en Bit[4]: first_channel_en Bit[3:2]: Not used Bit[1]: auto_first_en Bit[0]: br_first
P2:0x5F	BIST	0x00	RW	Bit[7:1]: Not used Bit[0]: BIST
P2:0xA0	DEM_V_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Image vertical start[10:8]
P2:0xA1	DEM_V_START_8LSB	0x00	RW	Bit[7:0]: Image vertical start[7:0]
P2:0xA2	DEM_V_SIZE_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Image vertical size[10:8]
P2:0xA3	DEM_V_SIZE_8LSB	0x40	RW	Bit[7:0]: Image vertical size[7:0]

table 5-3 ISP registers (sheet 3 of 3)

address	register name	default value	R/W	description
P2:0xA4	DEM_H_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Image horizontal start[10:8]
P2:0xA5	DEM_H_START_8LSB	0x00	RW	Bit[7:0]: Image horizontal start[7:0]
P2:0xA6	DEM_H_SIZE_3MSB	0x07	RW	Bit[7:3]: Not used Bit[2:0]: Image half horizontal size[10:8]
P2:0xA7	DEM_H_SIZE_8LSB	0x88	RW	Bit[7:0]: Image half horizontal size[7:0]
P2:0xF9	DC_TEST_EN, DC_MIST_SET, DC_DATA_SET_L2	0x00	RW	Bit[7:6]: Not used Bit[5]: Enable test pad Bit[4]: Test VSYNC pad Bit[3]: Test HSYNC pad Bit[2]: Not used Bit[1]: Test data pad[1] Bit[0]: Test data pad[0]
P2:0xFA	DC_DATA_SET_H8	0x00	RW	Bit[7:0]: Test data pad[9:2]

5.4 DAC code [P3:0x0E]

table 5-4 DAC code register

address	register name	default value	R/W	description
P3:0x0E	BIN_C_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: bin_c_en

5.5 OTP [P6:0x00 - P6:0x2F, P6:0xFD]

table 5-5 OTP registers (sheet 1 of 2)

address	register name	default value	R/W	description
P6:0x00~ P6:0x1F	OTP_DATA	0x00	RW	If OTP_PGM_EN = 1'b1: Program OTP Address0 Data If OTP_PGM_EN = 1'b0: Read OTP Address0 Data (read only)
P6:0x20	OTP_EF_PGM_STATE	–	R	OTP Program State

table 5-5 OTP registers (sheet 2 of 2)

address	register name	default value	R/W	description
P6:0x21	OTP_ PGM_EN	0x00	RW	OTP Program and Read Mode Select 0: Read mode 1: Program mode
P6:0x22	OTP_ PGM_ADDRESS	0x11	RW	OTP Single Mode Program Address
P6:0x23	OTP_ PGM_DATA	0x00	RW	OTP Single Mode Program Data
P6:0x24~ P6:0x29	RSVD	–	–	Reserved
P6:0x2A	OTP_ TMAX_PGM_8MSB	0x01	RW	Bit[7:0]: OTP PGM 1 byte max high 8 bits
P6:0x2B~ P6:0x2D	RSVD	–	–	Reserved
P6:0x2E	OTP_ PGM_START	0x00	RW	OTP Program Start Bit[7:4]: Not used Bit[3]: Program batch start Bit[2]: Program chip batch start (only address[8:0]) Bit[1]: Program user batch start (only address[31:9]) Bit[0]: Single program start
P6:0x2F	OTP_ READ_LOAD	0x00	RW	OTP Load Data Enable
P6:0xFD	PAGE_FLAG	–	R	OTP Page Flag

6 operating specifications

6.1 absolute maximum ratings

table 6-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 functional temperature

table 6-2 functional temperature

parameter	range
operating temperature (for applications up to 90 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	-20°C to +60°C junction temperature

a. sensor functions, but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

6.3 DC characteristics

table 6-3 DC characteristics (-30°C < T_J < 85°C)[ab]

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	3.0	V
V_{DD-D}	supply voltage (digital core)	1.35	1.5	1.65	V
V_{DD-IO}	supply voltage (digital I/O)	1.7 (2.6)	1.8 (2.8)	1.98 (3.0)	V
I_{DD-A}			TBD		mA
I_{DD-D}	active (operating) current		TBD		mA
I_{DD-IO}			TBD		mA
digital inputs (typical conditions: DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SCL and SDA			0.54	V
V_{IH}[c]	SCL and SDA	1.26			V

a. external clock is stopped during measurement

b. standby current is based on room temperature

c. based on DOVDD = 1.8V

6.4 timing characteristics

figure 6-1 reference clock input timing diagram

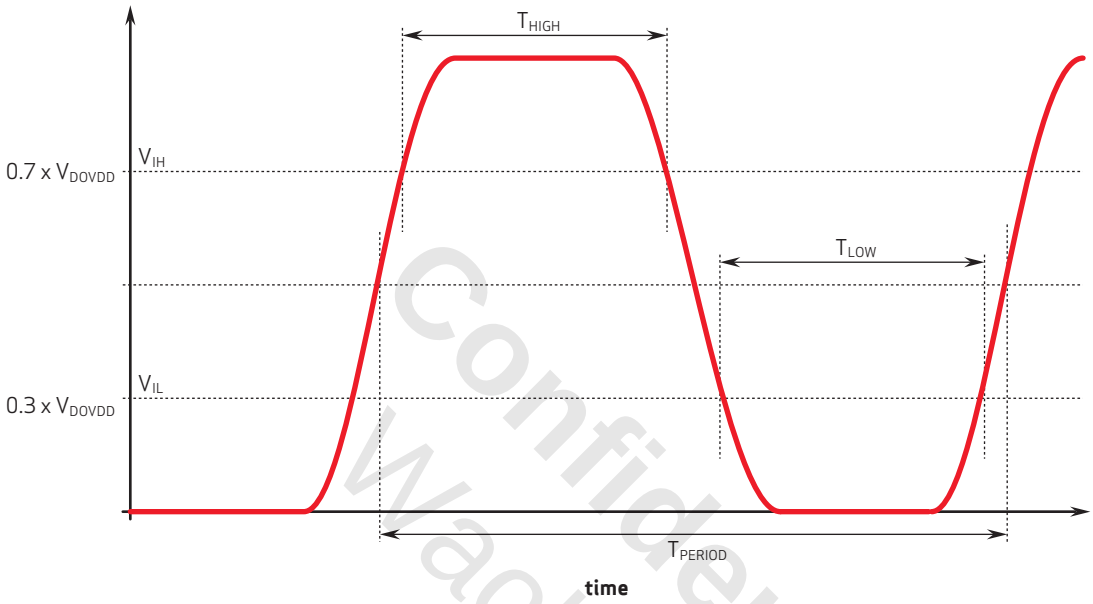


table 6-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
ECLK	frequency (ECLK)	10	24	36	MHz
V_{CLK}	ECLK amplitude	1.7/2.7	1.8/2.8	1.9/3.0	V
T_{HIGH}/T_{LOW}	ECLK duty cycle	$0.4\times T_{PERIOD}$	$0.5\times T_{PERIOD}$	$0.6\times T_{PERIOD}$	ns
T_{PERIOD}	ECLK period	27.78	41.66	100	ns

7 mechanical specifications

7.1 physical specifications

figure 7-1 package specifications

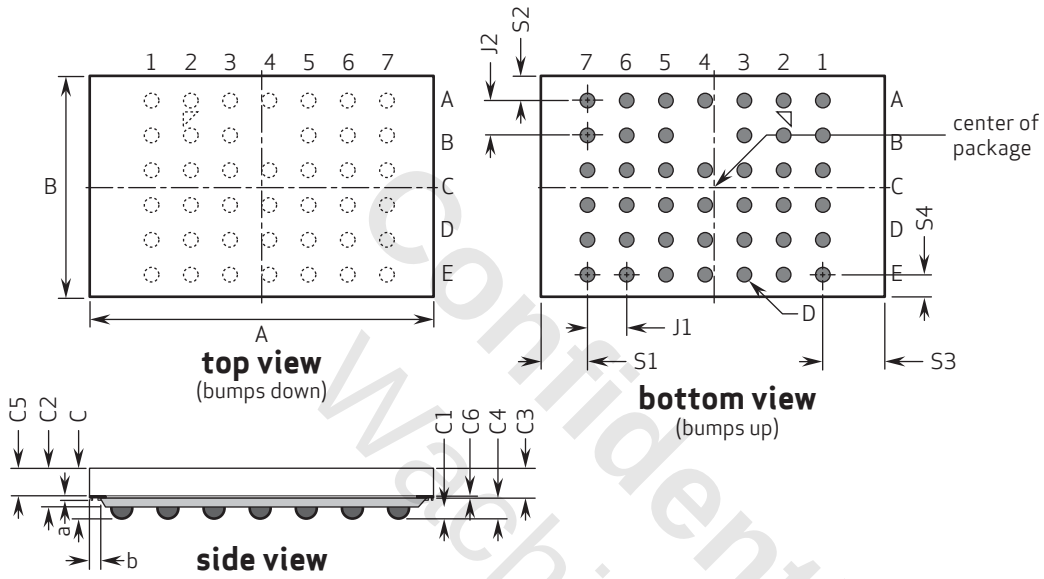


table 7-1 package dimensions (sheet 1 of 2)

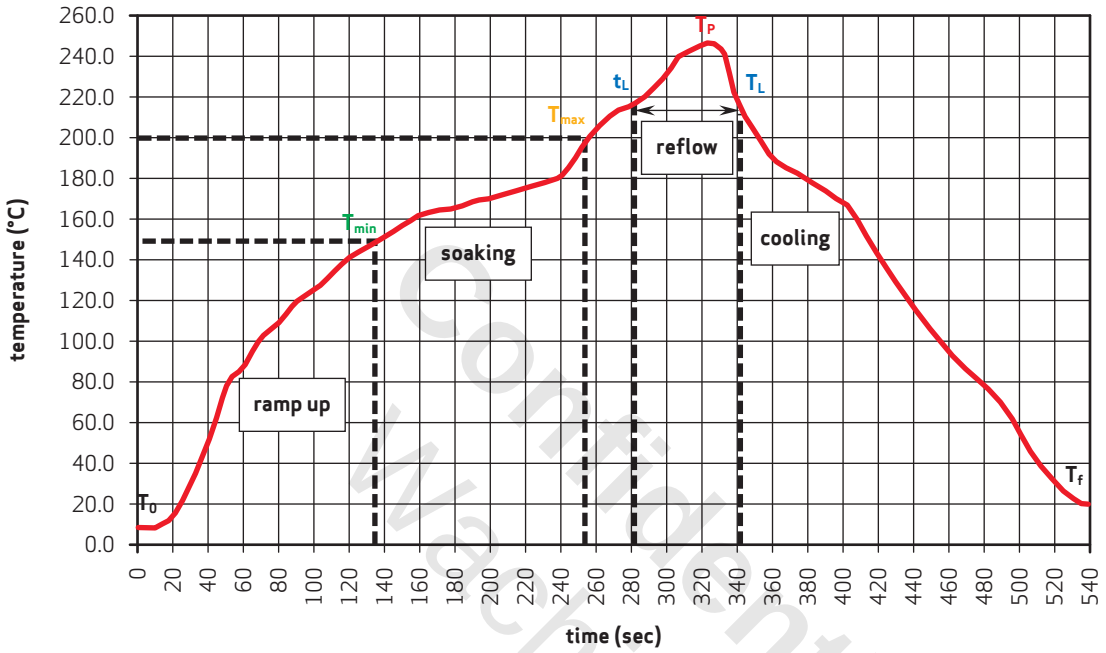
parameter	symbol	min	typ	max	unit
package body dimension x	A	6426	6451	6476	µm
package body dimension y	B	4154	4179	4204	µm
package height	C	585	640	695	µm
ball height	C1	100	130	160	µm
package body thickness	C2	480	510	540	µm
thickness from top glass surface to die	C3	330	345	360	µm
image plane height	C4	250	295	340	µm
glass thickness	C5	290	300	310	µm
air gap between sensor and glass	C6	41	45	49	µm
ball diameter	D	220	250	280	µm
total pin count	N		41		

table 7-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
pin count x-axis	N1		7		
pin count y-axis	N2		6		
pins pitch x-axis	J1	720	730	740	µm
pins pitch y-axis	J2	640	650	660	µm
edge-to-pin center distance along x1	S1	850.7	880.695	910.7	µm
edge-to-pin center distance along y1	S2	428.2	458.235	488.2	µm
edge-to-pin center distance along x2	S3	1160.3	1190.305	1220.3	µm
edge-to-pin center distance along y2	S4	440.8	470.765	500.8	µm
edge-to-trench bottom opening distance along x	a	30	50	70	µm
edge-to-trench bottom opening distance along y	b	126	146	166	µm

7.2 IR reflow specifications

figure 7-2 IR reflow ramp rate requirements



note The OS02G10 uses a lead-free package.

note To reduce image artifacts from infrared light and to provide the best image quality. OmniVision recommends an IR cut filter.

table 7-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5° (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30~120 seconds
ramp down A (T_P to T_L)	cooling down from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling down from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

a. maximum number of reflow cycles = 3

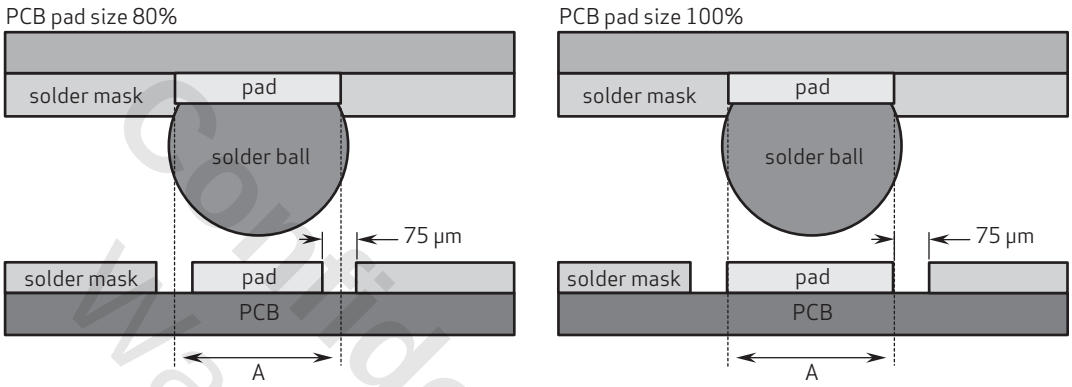
b. N2 gas reflow or control O2 gas PPM <500 as recommendation

7.3 PCB and SMT design recommendations

7.3.1 PCB design recommendations

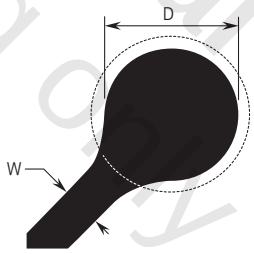
- solder pad of PCB: non solder mask defined (NSMD)
- PCB pad size: 80%~100% (90% ± 10%) of package's ball pad opening
- gap between pad to neighboring solder mask: 75 µm (minimum)

figure 7-3 PCB pad example



- trace width: must be less than 1/2 ball diameter (W<1/2 D)
- recommend adding tear drop design on trace connecting to via and pad

figure 7-4 tear drop design example



- PCB material: high performance FR4 with high Tg and low CTE substrate material is recommended
- package edge to PCB edge minimum 1.0 mm is recommended

table 7-3 ball pad opening size and recommended PCB NSMD ball pad size

device name	package type	package size	CSP/BGA ball pad opening size	recommended PCB NSMD ball pad size
OS02G10	CSP	6.451 mm × 4.179 mm	250 µm	225 µm ± 25 µm

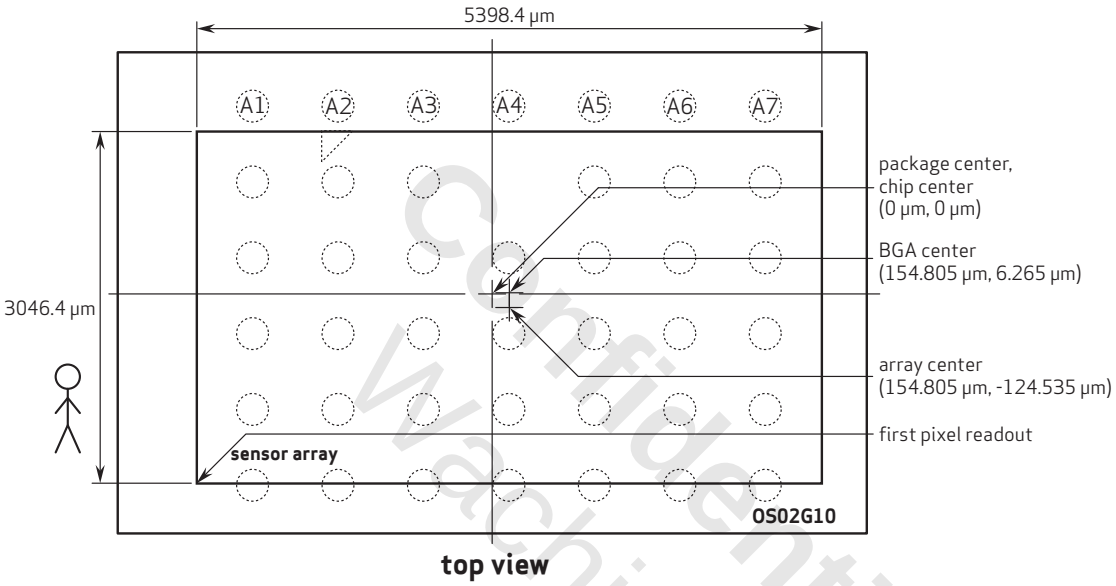
7.3.2 SMT design recommendations

- stencil: laser cut with electro-polishing
- stencil opening: 90~100% of PCB pad size
- stencil thickness: 0.08~0.15 mm
- solder material: SAC 305 is recommended
- solder paste: type 4 (20 µm to 38 µm) or finer solder sphere particle size is recommended
- SMT profile: refer to solder paste datasheet and product datasheet

8 optical specifications

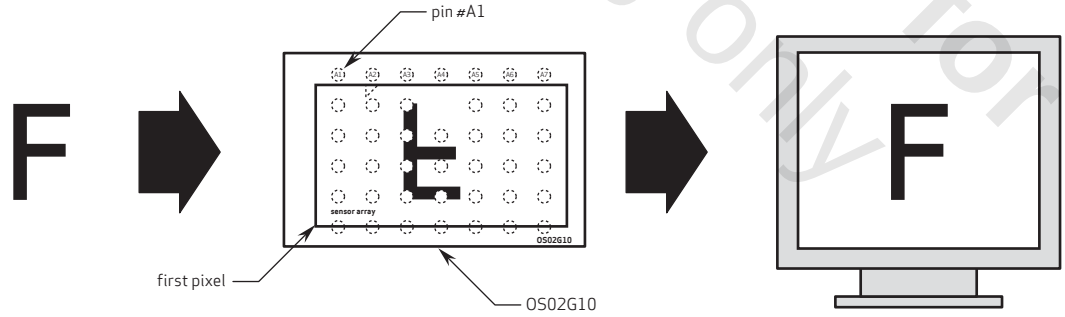
8.1 sensor array center

figure 8-1 sensor array center



note this drawing is not to scale and is for reference only.

figure 8-2 final image output



8.2 lens chief ray angle (CRA)

figure 8-3 chief ray angle (CRA)

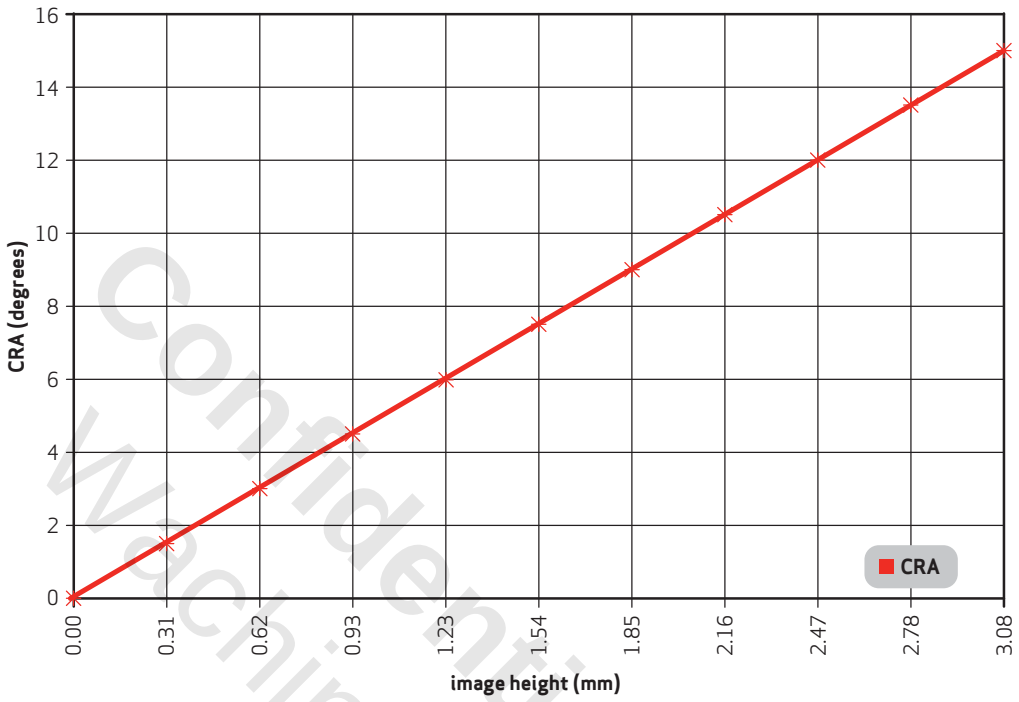


table 8-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0	0.00	0.00
10	0.31	1.50
20	0.62	3.00
30	0.93	4.50
40	1.23	6.00
50	1.54	7.50
60	1.85	9.00
70	2.16	10.50
80	2.47	12.00
90	2.78	13.50
100	3.08	15.00

revision history

version 1.0 05.06.2020

- initial release

version 1.1 09.01.2020

- in features, changed third bullet to "supports output formats: 12-bit/10-bit RAW RGB" and changed sixth bullet to "supports DVP 12-bit output interface"
- in key specifications, added core power supply to power supply specification, added "(see sidebar note)" to power requirements specification, and changed image area specification to 6417 µm x 4145 µm
- in table 2-5, changed register name of register P0:0x44 to "MP_DA_SSEL, MP_CLK_SSEL, MP_PHASE_INV, MP_PHASE", changed description of register bit P0:0x44[4] to "mp_phase_inv, DPHY DDR clock phase inverted", and changed description of register bits P0:0x44[3:0] to "mp_phase"
- in section 2.7.2, changed first sentence of first paragraph to "A reset can also be initiated via the SCCB interface by writing P0:0x20 = 0x00."
- in table 2-6, changed register name of register P0:0x2F to "MPLL_NC", changed description of register bits P0:0x2F[2:0] to "mpll_mc, PLL output =[PLL input * (2- mpll_nc[7])...", changed register name of register P0:0x30 to "DPLL_CP_DIV, DPLL_DACCLK_DIV, MPLL_DIV", removed binary values for register bits P0:0x30[5:4], changed description of register bits P0:0x30[3:2] to "dpll_dacclk_div" and removed binary values, changed description of register bits P0:0x30[1:0] to "mpll_div" and removed binary values, changed register name of register P0:0x43 to "MP_RAW_SEL, MP_DOUBLE", changed description of register bits P0:0x43[2:1] to "mp_raw_sel", added binary value selections 00, 01, 10, and 11 for register bits P0:0x43[2:1], and changed description of register bit P0:0x43[0] to "mp_double"
- in figure 2-4, added Fout between PLL clock select and system clock blocks
- in table 4-2, changed register name of register P1:0x34 to "COL_ANA_ADDR_START_2MSB, COL_ANA_ADDR_SIZE_2MSB", changed description of register bits P1:0x34[5:4] to "Col_ana_addr_ size _2msb", changed description of register bits P1:0x34[1:0] to "Col_ana_addr_start_2msb", changed register name of register P1:0x35 to "COL_ANA_ADDR_START_8LSB", changed description of register bits P1:0x35[7:0] to "Col_ana_addr_start_8lsb", changed register name of register P1:0x36 to "COL_ANA_ADDR_SIZE_8LSB", and changed description of register bits P1:0x36[1:0] to "Col_ana_addr_ size _8lsb"
- in chapter 4, moved sections 4.4.1 and 4.4.2 immediately after figure 4-4
- in section 4.4.1, added sixth sentence to first paragraph, changed second sentence of fourth paragraph to "The digital gain registers are P1:0x37 and P1:0x39.", changed third sentence of fourth paragraph to "P1:0x39 = 0x40 is 1x digital gain.", and changed fourth sentence of fourth paragraph to "Maximum digital gain is (P1:0x37 = 0x07, P1:0x39 = 0xFF) = 32x."
- in table 4-3, changed description of register bit P1:0x0B[6] to "exter_frame_num_x256_en, When enabled, 1 LSB of exter_sync_frame_num (P1:0x17)...", changed description of register bit P1:0x0B[4] to "exter_sync_manual_en, Configure a posedge in this bit to trigger a sync output in master mode", changed description of register bit P1:0x0B[3] to "exter_sync_auto_en, Sensor in master mode will send sync signal every exter_sync_frame_num (P1:0x17) frames automatically", changed description of register bit P1:0x0B[2] to "sync_no_wait_en", removed binary value

selections for register bit P1:0x0B[1], and changed description of register bit P1:0x0B[0] to "External sync master mode"

- in table 4-5, changed register name of register P1:0xFA to "ABL_TRIGGER", changed description of register bit P1:0xFA[7] to "Manual function, Use with bit[0] at same time", changed description of register bit P1:0xFA[5] to "Auto BLC enable", changed description of register bit P1:0xFA[4] to "RPC function", changed description of register bit P1:0xFA[3] to "Exp function", changed description of register bit P1:0xFA[2] to "Mean function", changed description of register bit P1:0xFA[1] to "frame_count reset", and changed description of register bit P1:0xFA[0] to "Manual function"
- in table 4-6, changed register name of register P1:0xF0 to "GB_SUBOFFSET", changed description of register bits P1:0xF0[7:0] to "Blacklevel offset, Gb channel, low 8 bits, Total register is 9 bits with MSB...", changed register name of register P1:0xF1 to "BLUE_SUBOFFSET", changed description of register bits P1:0xF1[7:0] to "Blacklevel offset, Blue channel, low 8 bits, Total register is 9 bits with MSB...", changed register name of register P1:0xF2 to "RED_SUBOFFSET", changed description of register bits P1:0xF2[7:0] to "Blacklevel offset, Red channel, low 8 bits, Total register is 9 bits with MSB...", changed register name of register P1:0xF3 to "GR_SUBOFFSET", and changed description of register bits P1:0xF3[7:0] to "Blacklevel offset Gr channel, low 8 bits, Total register is 9 bits with MSB..."
- in table 5-1, changed register name of register P0:0x2E to "MPLL_NC", changed description of register bits P0:0x2E[7:0] to "mpll_nc", changed register name of register P0:0x2F to "MPLL_NC", changed description of register bits P0:0x2F[7:0] to "mpll_mc, PLL output =[PLL input * (2-mpll_nc[7])...", changed register name of register P0:0x30 to "DPLL_CP_DIV, DPLL_DACCLK_DIV, MPLL_DIV", removed binary values for register bits P0:0x30[5:4], changed description of register bits P0:0x30[3:2] to "dpll_dacclk_div" and removed binary values, changed description of register bits P0:0x30[1:0] to "mpll_div" and removed binary values, changed register name, default value, and R/W of register P0:0x33 to "DPLL_BIAS", "0x01", and "RW", respectively, changed description of register bit P0:0x33[7:3] to "Not used", changed description of register bit P0:0x33[2:0] to "dpll_bias, PLL chargepump current control", changed register name, default value, R/W, and register description title of register P0:0x35 to "DPLL_DCTL, MPLL_BIAS, MPLL_DCTL", 0x02, and RW, respectively, changed description of register bits P0:0x35[7:5] to "Not used", changed description of register bit P0:0x35[4] to "dpll_dctl, Choose PLL's PFD delay time to remove dead zone", changed description of register bit P0:0x35[3:1] to "mpll_bias, PLL chargepump current control", changed description of register bit P0:0x35[0] to "mpll_dctl, Choose PLL's PFD delay time to remove dead zone", changed binary value selection 0 description to "Disable PCLK gating" for register bit P0:38[4], changed binary value selection 1 description to "Enable PCLK gating" for register bit P0:38[4], changed binary value selection 0 description to "Disable PCLK gating" for register bit P0:38[0], changed binary value selection 1 description to "Enable PCLK gating" for register bit P0:38[0], changed register name of register P0:0x41 to "DPLL_NC", changed description of register bits P0:0x41[7:6] to "Not used", changed description of register bits P0:0x41[5:0] to "dpll_nc", changed register name of register P0:0x41 to "DPLL_NC", changed register name of register P0:0x42 to "DPLL_MC", changed description of register bits P0:0x42[7:2] to "Not used", changed description of register bits P0:0x42[1:0] to "dpll_mc, PLL output = [PLL input * (pll_nc+3)...", changed register name of register P0:0x43 to "MP_RAW_SEL, MP_DOUBLE", changed description of register bits P0:0x43[7:3] to "Not used", changed description of register bits P0:0x43[2:1] to "mp_raw_sel", added binary value selection 00, 01, 10, and 11 for register bits P0:0x43[2:1], changed description of register bit P0:0x43[0] to "mp_double", changed register name of register P0:0x44 to "MP_DA_SSEL, MP_CLK_SSEL, MP_PHASE_INV, MP_PHASE", changed description of register bit P0:0x44[4] to "mp_phase_inv, DPHY DDR clock phase inverted", and changed description of register bits P0:0x44[3:0] to "mp_phase"
- in table 5-2, changed description of register bit P1:0x0B[6] to "exter_frame_num_x256_en, When enabled, 1 LSB of exter_sync_frame_num (P1:0x17)...", changed description of register bit P1:0x0B[4] to "exter_sync_manual_en, Configure a posedge in this bit to trigger a sync output in master mode", changed description of register bit P1:0x0B[3] to "exter_sync_auto_en, Sensor in master mode will send sync signal every exter_sync_frame_num (P1:0x17) frames automatically",

changed description of register bit P1:0x0B[2] to "sync_no_wait_en", removed binary value selections for register bit P1:0x0B[1], changed description of register bit P1:0x0B[0] to "External sync master mode", changed register name of register P1:0x34 to "COL_ANA_ADDR_START_2MSB, COL_ANA_ADDR_SIZE_2MSB", changed description of register bits P1:0x34[5:4] to "Col_ana_addr_ size _2msb", changed description of register bits P1:0x34[1:0] to "Col_ana_addr_start_2msb", changed register name of register P1:0x35 to "COL_ANA_ADDR_START_8LSB", changed description of register bits P1:0x35[7:0] to "Col_ana_addr_start_8lsb", changed register name of register P1:0x36 to "COL_ANA_ADDR_SIZE_8LSB", changed description of register bits P1:0x36[7:0] to "Col_ana_addr_ size _8lsb", changed default value of register P1:0x37 to "0x00", changed description of register bits P1:0x37[7:3] to "Not used", changed description of register bits P1:0x37[2:0] to "Dig_gain[10:8]", changed description of register bits P1:0x39[7:0] to "Global digital gain(0x37:39, 1x~32x)[7:0]...", changed register name, default value, and R/W of register P1:0x46 to "DC_LEVEL_LIMIT_EN", "0x00", and "RW", respectively, changed description of register bits P1:0x46[7:1] to "Not used", changed description of register bit P1:0x46[0] to "Dc_level_limit_en ", changed register name, default value, and R/W of register P1:0x47 to "DC_LEVEL_LIMIT", "0x20", and RW, respectively, changed description of register bits P1:0x47[7:0] to "Limitation of DC", changed register name, default value, and R/W of register P1:0x48 to "BLC_DATA_LIMIT", "0xE8", and RW, respectively, changed description of register bits P1:0x48[7:0] to "Limitation of data output", changed register name, default value, and R/W of register P1:0x49 to "BLC_DATA_LIMIT[13:12], DC_LEVEL_LIMIT[10:8]", "0x33", and RW, respectively, changed description of register bits P1:0x49[7:6] to "Not used", changed description of register bits P1:0x49[5:4] to "Limitation of data output", changed description of register bit P1:0x49[3] to "Not used", changed description of register bits P1:0x49[2:0] to "Limitation of DC", changed register name of register P1:0xF0 to "GB_SUBOFFSET", changed description of register bits P1:0xF0[7:0] to "Blacklevel offset, Gb channel, low 8 bits, Total register is 9 bits with MSB...", changed register name of register P1:0xF1 to "BLUE_SUBOFFSET", changed description of register bits P1:0xF1[7:0] to "Blacklevel offset, Blue channel, low 8 bits, Total register is 9 bits with MSB...", changed register name of register P1:0xF2 to "RED_SUBOFFSET", changed description of register bits P1:0xF2[7:0] to "Blacklevel offset, Red channel, low 8 bits, Total register is 9 bits with MSB...", changed register name of register P1:0xF3 to "GR_SUBOFFSET", changed description of register bits P1:0xF3[7:0] to "Blacklevel offset, Gr channel, low 8 bits, Total register is 9 bits with MSB...", changed register name of register P1:0xFA to "ABL_TRIGGER", changed description of register bit P1:0xFA[7] to "Manual function, Use with bit[0] at same time", changed description of register bit P1:0xFA[6] to "Not used", changed description of register bit P1:0xFA[5] to "Auto BLC enable", changed description of register bit P1:0xFA[4] to "RPC function", changed description of register bit P1:0xFA[3] to "Exp function", changed description of register bit P1:0xFA[2] to "Mean function", changed description of register bit P1:0xFA[1] to "frame_count reset", changed description of register bit P1:0xFA[0] to "Manual function", changed description of register bit P1:0xFB[6] to "blc_test_en...", changed description of register bit P1:0xFB[3] to "ob2_en", and changed description of register bits P1:0xFB[2:1] to "blc_mode..."

- in table 6-4, changed min and max values for symbol T_{HIGH}/T_{LOW} to $0.4\times T_{PERIOD}$ and $0.6\times T_{PERIOD}$, respectively, and removed row for symbol tr/tf (10%~90%)

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- in table 1-3, changed symbol FSIN to EVSYNC
- in chapter 2, completely replaced figures 2-2 and 2-3
- in section 4.4.1, changed fifth line after fourth paragraph to "78 39 80 ;digital gain 2x"

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