

WPT2N31

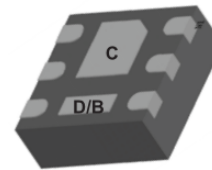
Single, PNP, -30V, -3A, Power Transistor with
20V N-MOSFET

[Http://www.sh-willsemi.com](http://www.sh-willsemi.com)

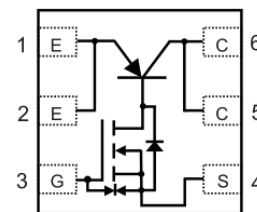
Descriptions

The WPT2N31 is PNP bipolar power transistor
with 20V N-MOSFET. This device is suitable for use
in charging circuit and other power management.

Standard Product WPT2N31 is Pb-free.



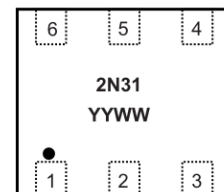
DFN2x2-6L



Pin configuration (Top view)

Features

- Ultra low collector-to-emitter saturation voltage
- High DC current gain >100
- 3A continue collector current
- Small package DFN2x2-6L



2N31 = Device Code
YY = Year
WW = Week

Marking

Order information

Device	Package	Shipping
WPT2N31-6/TR	DFN2*2-6L	3000/Reel&Tape

Applications

- Charging circuit
- Other power management in portable equipments

Absolute Maximum ratings

Parameter	Symbol	Value	Unit
PNP Transistor			
Collector-emitter voltage	V_{CEO}	-30	V
Collector-base voltage	V_{CBO}	-30	V
Emitter-base voltage	V_{EBO}	-6	V
Continuous collector current	I_C	-3	A
Pulse collector current	I_{CM}	-6	A
N-MOSFET			
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 6	V
Continuous Drain Current	I_D	1.7	A
Pulsed Drain Current ^a	I_{DM}	6	A
Power Dissipation and temperature			
Power dissipation	P_D	1.2	W
Junction Temperature	T_J	150	°C
Lead Temperature	T_L	260	°C
Storage Temperature Range	T_{stg}	-55~155	°C

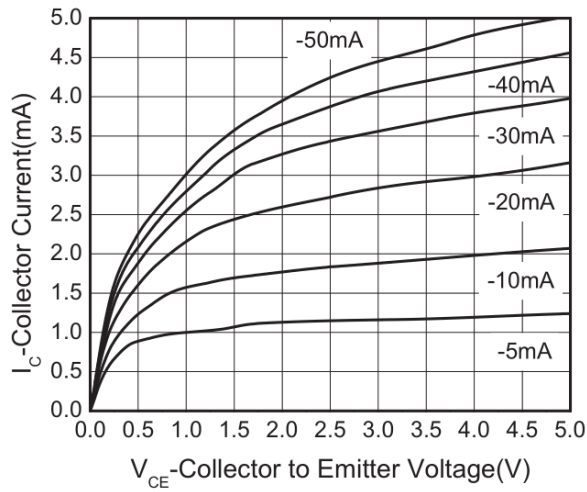
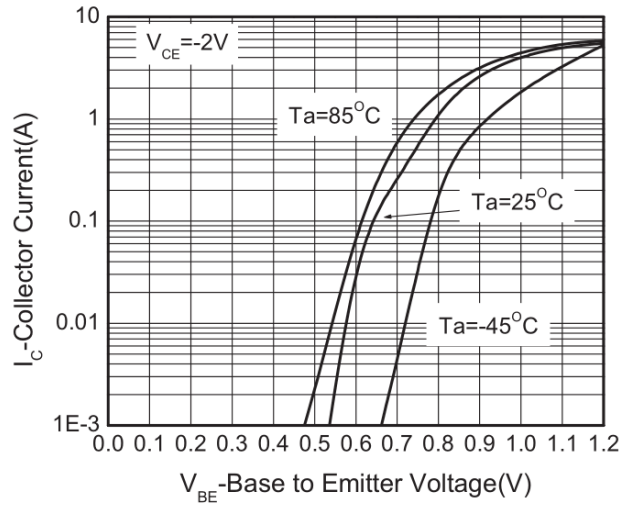
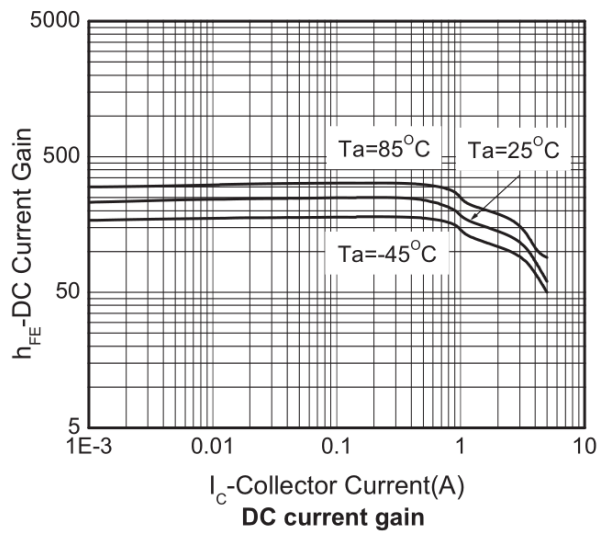
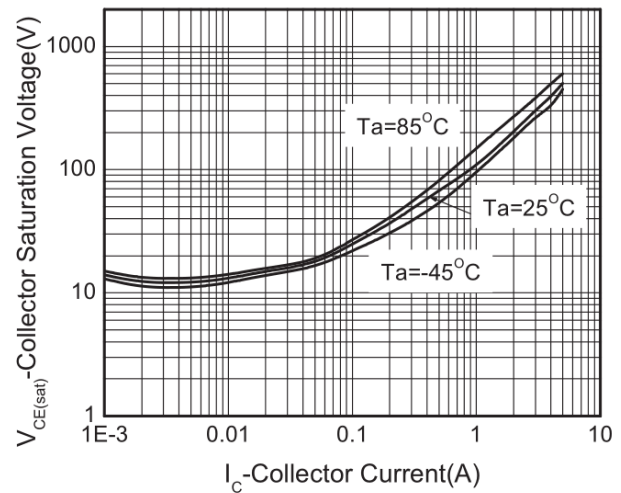
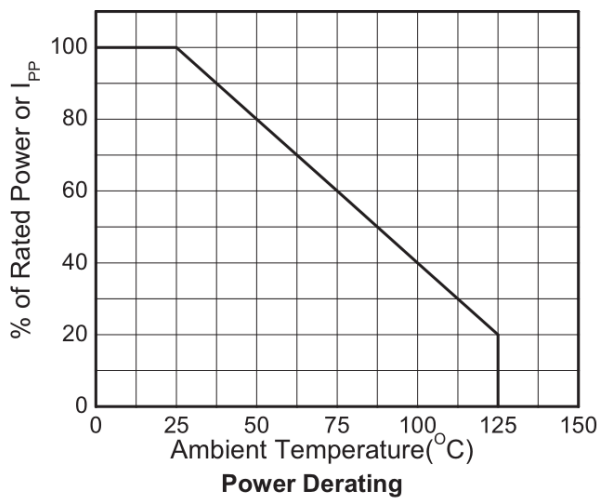
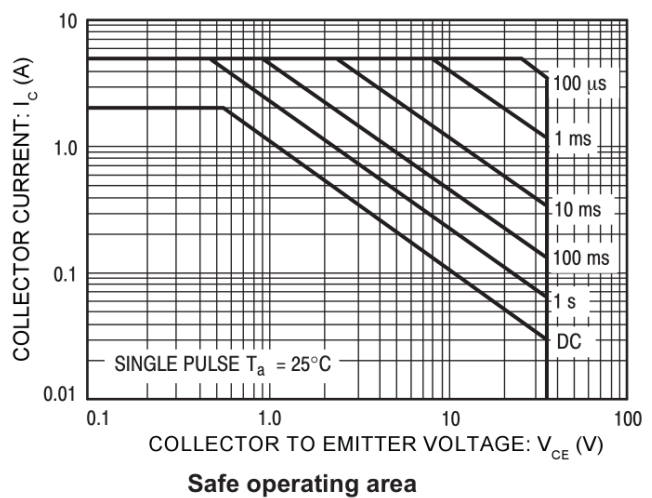
Thermal resistance ratings

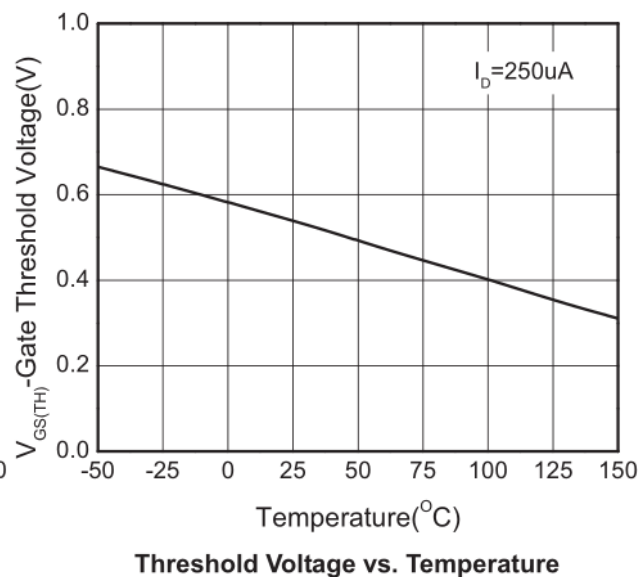
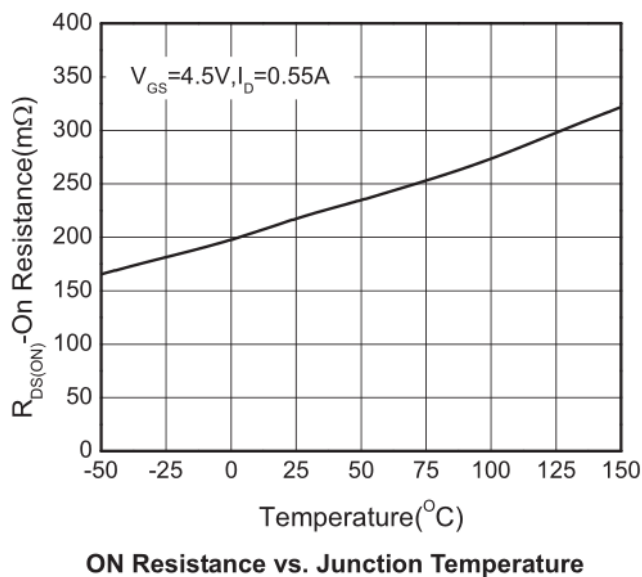
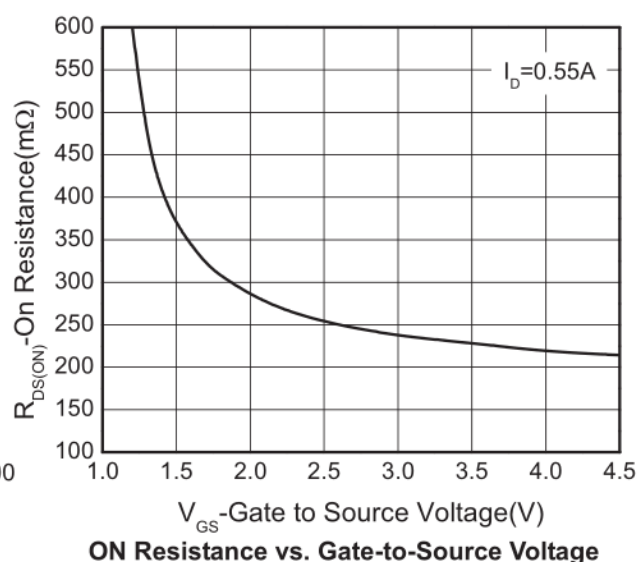
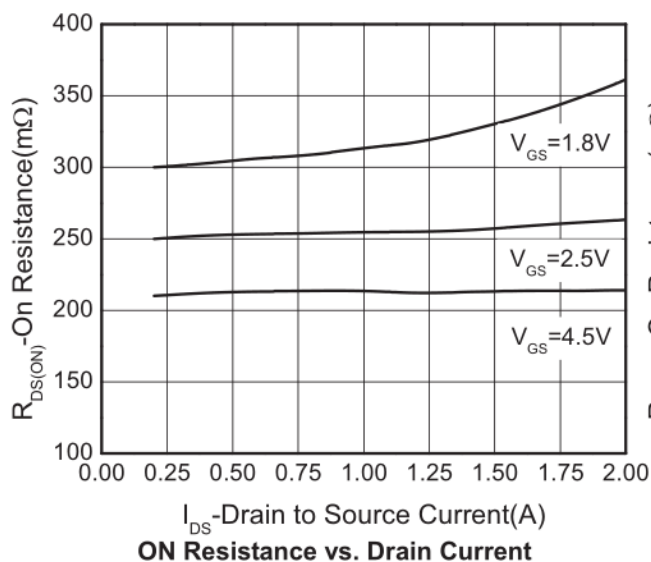
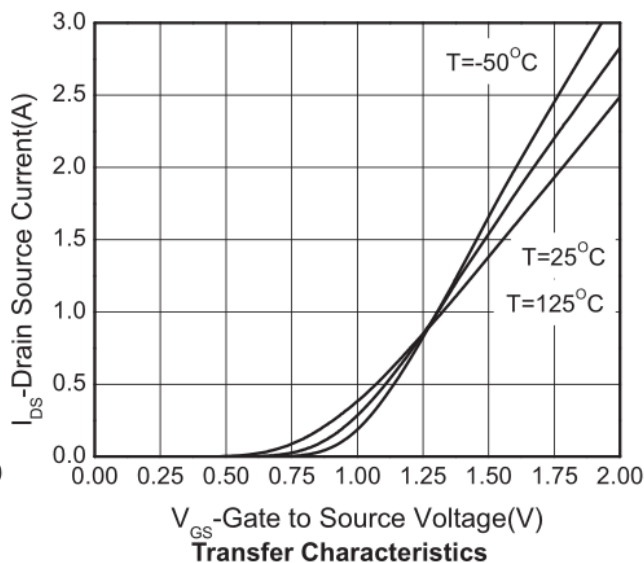
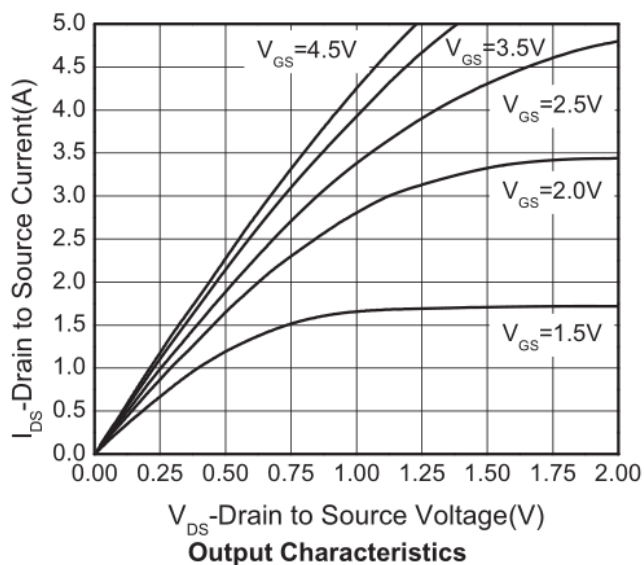
Parameter	Symbol	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	104	°C/W

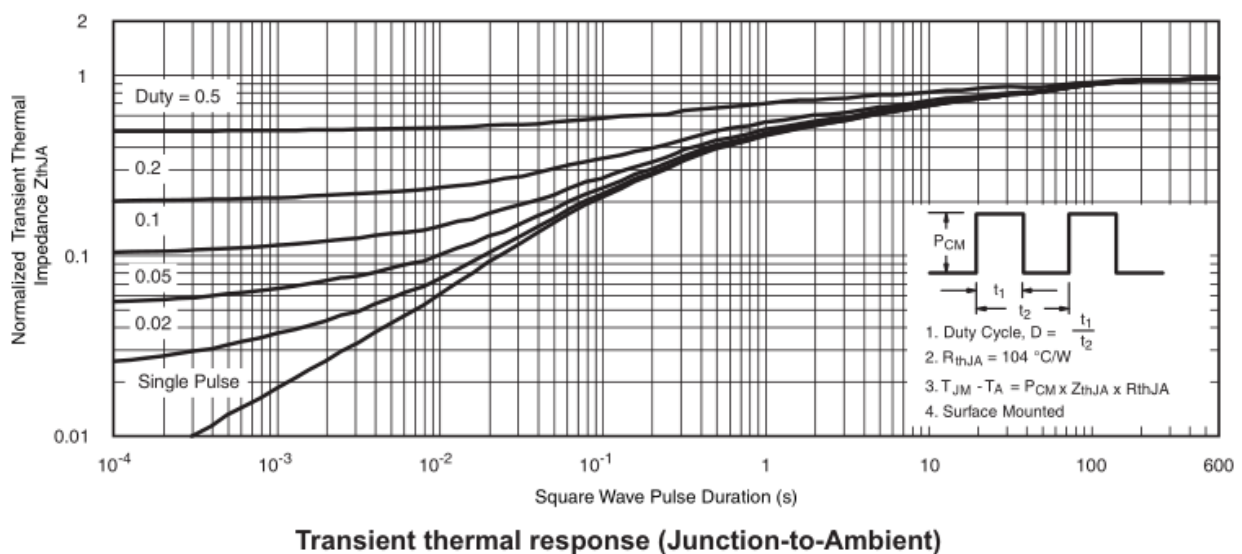
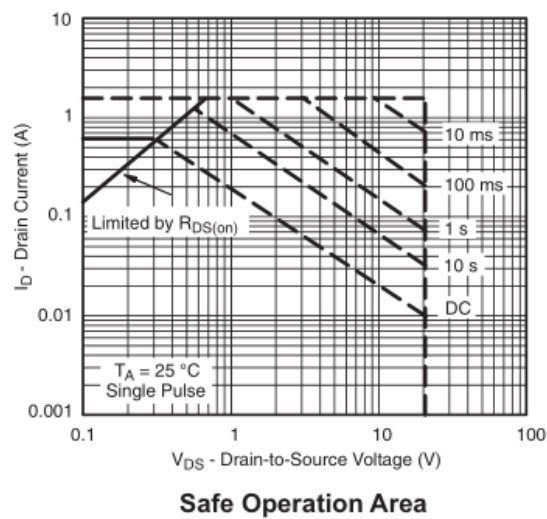
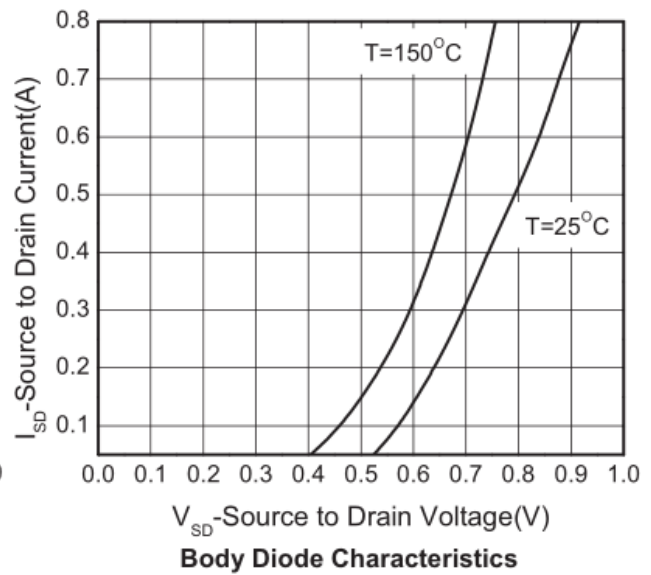
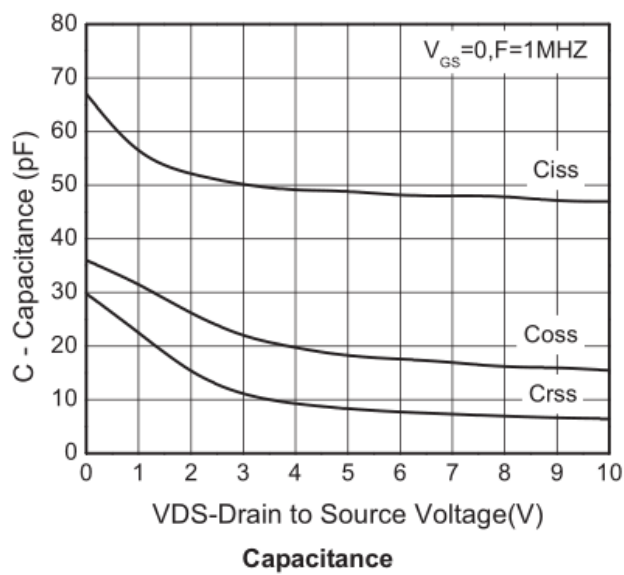
- a Pulse width=300μs, Duty Cycle<2%
- b Maximum junction temperature $T_J = 150^{\circ}\text{C}$

Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PNP Transistor						
Collector-emitter breakdown voltage	BV_{CEO}	$I_C = -10mA, I_B = 0mA$	-30			V
Collector-base breakdown voltage	BV_{CBO}	$I_C = -1mA, I_E = 0mA$	-30			V
Emitter-base breakdown voltage	BV_{EBO}	$I_E = -100uA, I_C = 0mA$	-6			V
Collector cutoff current	I_{CBO}	$V_{CB} = -30V$			-100	nA
Emitter cutoff current	I_{EBO}	$V_{EB} = 5V$			-100	nA
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -2A, I_B = -200mA$		-200	-400	mV
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = -2A, I_B = -200mA$		-1	-1.5	V
Base-emitter forward voltage	$V_{BE(on)}$	$I_C = -0.5A, V_{CE} = -2V$		-0.7	-1.0	V
DC current gain	HFE	$I_C = -1A, V_{CE} = -2V$	100		300	
N-MOSFET						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250uA$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$			1	μA
Gate –Source leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 5V$			± 5	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250uA$	0.45	0.55	1.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 0.55A$		220	260	m Ω
		$V_{GS} = 2.5V, I_D = 0.45A$		260	310	m Ω
		$V_{GS} = 1.8V, I_D = 0.35A$		320	380	m Ω
		$V_{GS} = 1.5V, I_D = 0.10A$		600	1100	m Ω
Input Capacitance	C_{iss}	$V_{DS} = 10V,$		50		pF
Output Capacitance	C_{oss}	$V_{GS} = 0V,$		13		pF
Reverse Transfer Capacitance	C_{rss}	$F = 1Mhz$		8		pF
Total Gate Charge	$Q_{G(TOT)}$	$V_{DS} = 10V,$ $V_{GS} = 4.5V,$ $I_D = 0.6A$		1.15		nC
Threshold gate charge	$Q_{G(TH)}$			0.06		nC
Gate-Source Charge	Q_{GS}			0.15		nC
Gate-Drain Charge	Q_{GD}			0.23		nC
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10V, V_{GS} = 4.5V,$ $I_D = 0.5A,$ $R_L = 10\Omega, R_G = 6\Omega$		22		ns
Turn-On Rise Time	t_r			80		ns
Turn-Off Delay Time	$t_{d(off)}$			700		ns
Turn-Off Fall Time	t_f			650		ns
Body Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 0.35A$	0.5	0.7	1.0	V

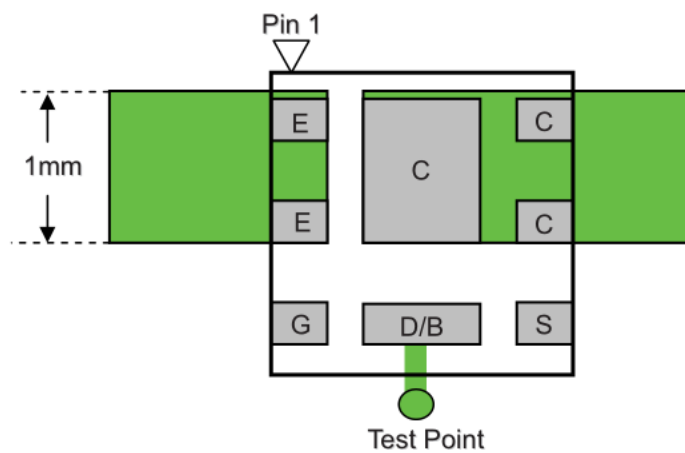
Typical Characteristics (Ta=25°C, unless otherwise noted)
PNP Transistor

Output characteristics

Transfer characteristics

DC current gain

C-E saturation voltage vs. Collector current

Power Derating

Safe operating area

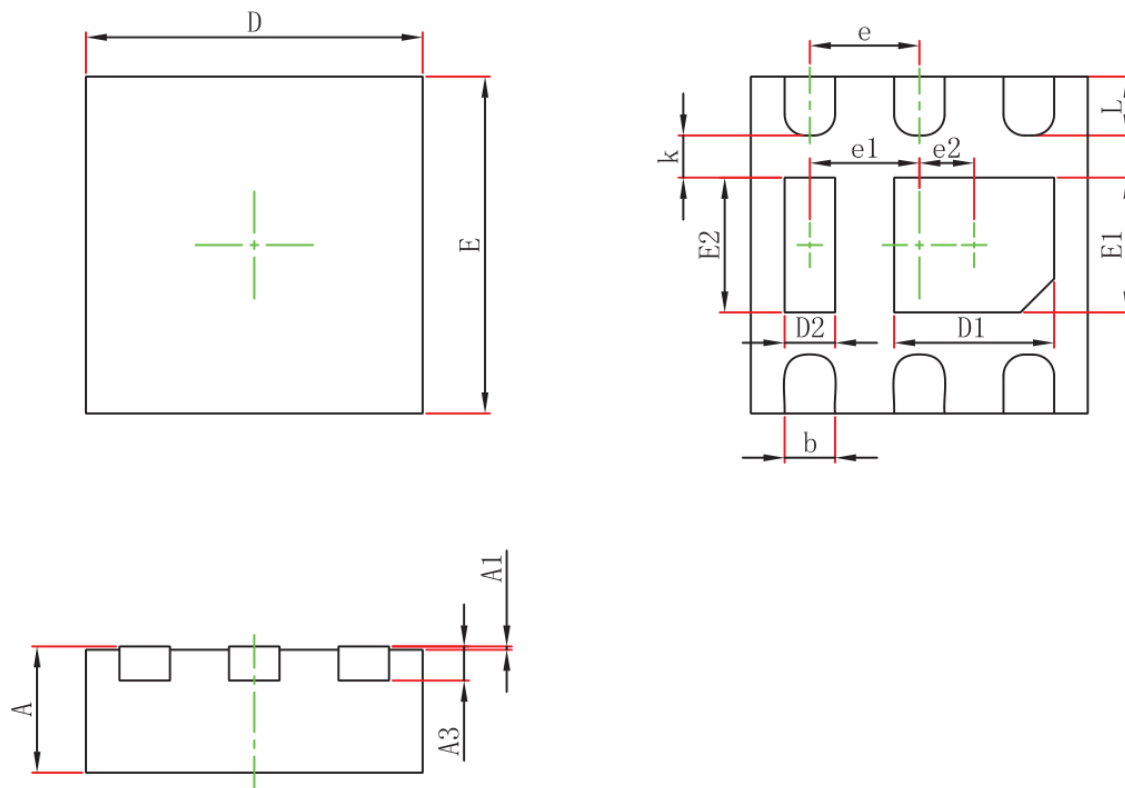
N-MOSFET




Application note and recommend layout

1. The greater exposed pad of bottom is connected to collector of transistor internally.
2. The smaller exposed pad of bottom is connected to drain of MOSFET and base of transistor internally.
3. Recommend layout as below:



Package outline dimensions
DFN2x2-6L


Symbol	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.700		0.800
A1	0.000		0.050
A3	0.203 Ref.		
D	1.924	2.000	2.076
E	1.924	2.000	2.076
D1	0.850	0.950	1.050
E1	0.700	0.800	0.900
D2	0.200	0.300	0.400
E2	0.700	0.800	0.900
e1	0.650 Typ.		
e2	0.325 Typ.		
k	0.200 Min.		
b	0.250	0.300	0.350
e	0.650 Typ.		
L	0.300	0.350	0.400